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Design Paradigm for Power Electronics based DC Distribution Systems

Harish Suryanarayana, *Member, IEEE*, and Scott D. Sudhoff, *Fellow, IEEE*

***Abstract*—The design of a dc distribution system is posed as an optimization problem which simultaneously utilizes time-domain analysis, distortion analysis, and stability analysis. The complete power distribution system is taken into consideration in the design process, capturing the interaction between various system components. Multi-objective optimization of mass and power loss metrics subject to transient performance constraints, distortion (voltage and current ripple constraints), and stability constraints is carried out in the proposed design paradigm. This provides an organized framework for the design of dc power distribution systems. The approach is demonstrated through the design of a representative system which consists of a generation system, two isolating peak current controlled dc-dc converter modules, and two constant power loads. A sample design is chosen and verified using a detailed waveform level simulation.**

***Index Terms*—power distribution, design optimization, power electronics, time domain analysis, stability analysis**

I. Introduction

With the advances in power electronics, dc power distribution systems are gaining popularity in a variety of applications. Some of these applications include shipboard power distribution systems [1-3], electric aircraft [4-6], hybrid electric vehicles [7, 8], wind energy collection systems [10-12] and solar farms [13-14]. In this work, the design requirements and the methodology used in the design of dc power distribution systems is investigated.

In a dc power distribution system, power is distributed between various system components through dc buses. These system components often include generation systems, DC-DC converters to change voltage levels and for fault mitigation and isolation, and various loads. Typically, each of these system components are designed separately. They are integrated to form the dc power distribution system at a later stage. This may lead to sub-optimal design from a system perspective.

A typical design process using various analyses is shown in Fig. 1. Each system requirement is sequentially tested and modifications are made to satisfy the requirements at each stage. However, modifications made at one stage can lead to requirements not being met at an earlier stage. This leads to a design spiral – wherein the analysis needs to be repeated several times. A more organized and time-efficient method is desirable.

An alternative design approach is proposed in this work, wherein analysis tools are recast as design tools and various system requirements are considered simultaneously. The design problem is posed as an optimization problem, wherein the function to be optimized takes into consideration time-domain requirements, distortion requirements, and stability requirements while minimizing metrics such as mass and power loss. This approach is shown in Fig. 2. Herein, various analysis tools are used to estimate the goodness of a design through the development of a fitness function. This fitness function formulation is then maximized in an evolutionary environment to obtain a Pareto-optimal front of designs from which a particular design can be chosen.

The difference between the traditional approach (Fig. 1) and the proposed approach (Fig. 2) is threefold. First, in the traditional approach, a viable solution is identified. However,

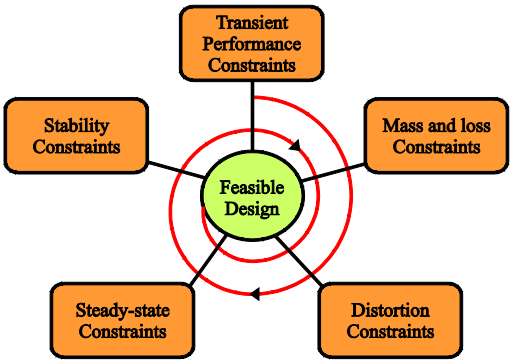

Fig. 1. Design spiral

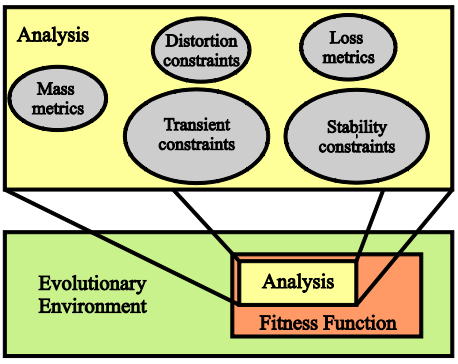

Fig. 2. Proposed design methodology

This work was submitted for review on June 13, 2016. This work was supported in part by the Office of Naval Research under grant – N000141410160. It was also supported in part by a fellowship from ABB Inc.

H. Suryanarayana was a graduate student in the Electrical and Computer Engineering department at Purdue University, W. Lafayette, IN – 47907, USA. Since 2014, he works as a research scientist at US Corporate Research Center, ABB Inc., Raleigh, NC – 27606, USA (e-mail: harish.suryanarayana@us.abb.com).

S. D. Sudhoff is the Michael and Katherine Birck Professor of Electrical and Computer Engineering at Purdue University, W. Lafayette, IN – 47907, USA, (e-mail: sudhoff@purdue.edu).

there is no direct effort at optimization in the formal sense, and the fundamental tradeoff between mass and loss (i.e. a Pareto-optimal front) is not identified. While the traditional approach yields a single design, the proposed approach yields a family of designs which span the trade-off between competing objectives. As an example, if system loss and mass were minimized, the result would be a family of designs, each of which have a different mass and loss, and also with the property that no design could be improved in terms of mass without increasing loss. From this the system designer could choose the design most compatible with platform needs. A second difference between methods is that in the traditional approach the engineer is highly involved in each step; in the proposed approach the role of the engineer is primarily in terms of identifying objectives and constraints. The proposed approach requires less engineering time, though more computing time. But given the low cost of high-performance computing, this is not a significant disadvantage. A disadvantage of the procedure may be that in removing the engineer from the design loop, less insight is obtained. However, given the choice between cost and performance, and insight; the former will generally be more desirable than the latter.

A precursor to the work presented here can be found in [15-17]. In [15], evolutionary computing is used for the design of the control gains in a power electronics based power system. Though the approach uses time-domain simulations for design, the focus is only on the control gains and not on the passive filter components. Also, distortion and stability requirements are not considered and the design space is much smaller. In [16], genetic algorithms are used in the design of the passive filters for harmonic compensation in offshore applications. In this case, the focus is only on the selection of the electrical value for passive filter components for minimizing the net rms current being drawn from the source – which translates to satisfying the distortion requirements. Again, the interaction between control gains and passives is not captured and the scope of the optimization is limited. In [17], a genetic algorithm based optimization is used to minimize the cost of the generation system. The novelty of the design methodology proposed herein lies in automatically capturing the interaction between the control and filter parameters in the complete system, while satisfying distortion, stability, and transient requirements, while minimizing metrics such as mass and power loss.

This paper is organized as follows. First, the design paradigm is presented Section II with the various analyses required and the formulation of the design problem as an optimization problem. A representative example system is described in Section III. In Section IV, a case study with the design paradigm as applied to the representative dc power distribution system presented. The results of the design optimization and validation are presented in Section V. A summary of the work and future research are set forth in Section VI.

II. DESIGN PARADIGM

The objective of this work is to establish an organized framework for the design of dc power distribution systems wherein the design problem is cast as an optimization problem. The first step is to define the design space. The system topology is assumed to be fixed beforehand based on application requirements. Lower level power electronics considerations such as the power semiconductors and gate drivers are assumed to be selected a-priori. Likewise the switching frequencies of the various components are assumed to be set based on semiconductor device limits. It is also assumed that each system component is connected to the dc bus through LC or LCL low-pass filters as is often the case [18-19]. Finally, it is assumed that the control paradigms (for example, in a simple case, a PI control) as well as the means to implement those controls have been selected.

The design space on this paradigm is focused on the passive elements and the local control gains. The first question which arises from this statement is why the semi-conductor and switching frequencies are not included. This extension is indeed possible and desirable. For this work, however, a scenario is considered wherein the components are built from standardized power switching blocks which include gate drive and other low-level controls optimized for a given frequency, and a computational platform for implementing controls, but not the passive elements which are left to be application specific. Such a platform would be an embodiment of the Power Electronic Building Block Concept [20]. This work focuses on the passive elements and local control gains of each component for not only do these design choices interact with each other within the component, but interact strongly with these features of every other component as well.

Consider a transient event such as large step decrease in load power. The overshoot in the bus voltage will depend on both the filter passives and control parameters. The impedance of each system component as seen from the bus is also dependent on both control gains and filter components. The stability of the system is affected by a change in either of them. Thus, a rigorous design methodology should involve the simultaneous choice of both the passives and the control gains for all components.

The various requirements specifications that typically need to be considered in a dc power distribution system are (a) mass and power loss metrics – reducing the mass and power loss are common design objectives [21], (b) transient specifications – these are the time-domain specifications detailing the dc bus current and voltage behavior during load changes and faults [22], (c) distortion specifications – these specifications address power quality of bus currents and voltages [23], and (d) stability specifications – to ensure that each system component of a dc power distribution system is stable on its own and as a part of an interconnected dc distribution system over a range of operating points [24].

Mass and power loss are important design considerations in power conversion systems. An isolated on board vehicle battery charger using SiC devices is presented in [25]. Close to 55% of the total mass of the charger system is due to passive

components (inductor, transformers and capacitors). In [26] it is seen that mass of the passives can contribute 25-50% of the total mass of the AC-AC conversion system depending on the topology chosen. Another large contributor to mass is the heat-sink, which in turn is designed based on the power loss in the system. Herein, the mass metric will be based on the mass of the passive components, because it is this portion of the mass that is different between the competing systems. Likewise, the power loss will focus on only inductive power loss, as this component of loss will be the chief differentiator between competing designs since with the problem as posed, switching losses will be relatively constant between different designs (power semiconductors and switching frequencies having been set a-priori). As, such, here the a-priori selection of switching device and frequencies allow the optimization in the context of what can be done with the chosen device. In order to, for example, compare system impact of SiC devices over Si devices, would require conducting two independent runs and then separately accounting for the differences in heat exchanger mass and losses. In such a comparison, the inductor loss model could potentially suffer from reduced fidelity in view of the potentially high switching frequencies.

In order to formulate the system design problem as an optimization problem, several analysis engines are required. These include:

(a) Average Value time-domain Model (AVM) – In this model, the non-linearities and primary time-domain dynamics of the currents and voltages are captured in a moving average sense. The state variables in this model are constant at steady state. A switching level simulation model or waveform level model (WLM) is more accurate than the AVM, but is computationally much more intensive and not as suitable for use in a design process. The AVM is ideally at least an order of magnitude faster than a simulation which includes switching dynamics. Time-domain behavior and interaction between system components is captured in the design process through the AVM.

(b) Distortion model – Since the AVM is used to capture the time-domain voltage and current dynamics, distortion information is unavailable in the design process. Thus a distortion analysis needs to be performed independently to evaluate power quality requirements. To this end, a distortion model of each system component will be used.

(c) Linear model – Small signal stability analysis using generalized immitance based stability methods [24] will be performed and included in the design process. To use this method, linear models of the system components obtained with an ideal current source load (to obtain source impedance) or an ideal voltage source input (to obtain load admittance) are required. These linear models can be derived from the AVMs of the system components.

For validation purposes, an additional model is developed:

(a) Waveform Level time-domain Model (WLM) – This is a detailed system representation which includes capturing the switching dynamics, at least in the sense of the dynamics of ideal switches. Because of this the computation time required to evaluate these models is high. The WLM has been developed for the representative system and the simulation results will be presented in Section V.

The analyses required have been set forth and the models for performing the analysis have been developed. Details of these analyses are set forth in [27]. The next step is the construction of the fitness function. Note that the focus of the design process is the selection of passive filter components and control gains. A design candidate can be thought of as a set of passive filter component parameters and control gains of all the system components in the dc power distribution system. The fitness function is a measure of goodness of a given design candidate. This measure is then used by the optimization engine to obtain viable optimal design candidates. Thus, the transient specifications, distortion specifications, stability specifications, mass and power loss metrics are all formulated and combined to form the fitness function, which is defined as

$$f = \begin{cases} \begin{bmatrix} \dfrac{1}{M_{pass}} \\ \dfrac{1}{P_{pass}} \end{bmatrix} & if\ c_{avg} = 1 \\ \begin{bmatrix} \varepsilon\left(c_{avg} - 1\right) \\ \varepsilon\left(c_{avg} - 1\right) \end{bmatrix} & if\ c_{avg} < 1 \end{cases} \tag{1}$$

where M_{pass} is the total mass of the inductors and capacitors and P_{pass} is the aggregate dc power loss in the inductors (the loss in the capacitors is neglected). The calculation of these quantities is set forth in Section IIA. Returning to (1), ε is a small positive number, and c_{avg} is the average constraint value. If all constraint are satisfied, the average constraint value is 1 (this will be discussed momentarily), and so the elements of the fitness vector are the reciprocal of mass, and the reciprocal of loss. An optimization engine that maximizes f will thus minimize mass and loss while maximizing their reciprocals.

To enforce constraints, the average constraint value is defined as

$$c_{avg} = \frac{\sum_{i=1}^{n_{con}} c_i}{n_{con}} \tag{2}$$

wherein n_{con} is the number of constraints, i is the i^{th} constraint and c_i is value between 0 and 1 which is defined based on each constraint imposed on the system. If the i^{th} constraint is satisfied, c_i equals 1. Otherwise, it is less than 1. Thus, if all the constraints are satisfied, then c_{avg} will be equal one. Otherwise, it will also take a value between 0 and 1. If some constraints are not satisfied, c_{avg} is less than 1 and the values of the fitness function are small negative numbers. The

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constraints themselves are discussed in Sections IIB through IID.

As a result of this formulation the fitness function has the following properties. Regardless of the system mass and loss, any design that is viable (all constraints met) will have a fitness values (both elements) which are larger (more favorable) than any system which is not viable (not all constraints met). Further, for non-viable systems, designs which are closer to viability have fitness vector elements which are more positive. For viable designs, the elements of the fitness vector improve as mass and loss are decreased. Most importantly, it should be observed that this formulation guarantees that all designs on the Pareto-optimal front will be in complete compliance with all constraints; otherwise the fitness value will be negative and the solution would not be in the non-dominated set of solutions and thus not be part of the solution set. A general discussion of the construction of fitness functions is set forth in [28].

An example of a function that may be used to assign a value to c_i is

$$\mathrm{lte}(x, x_{max}) = \begin{cases} 1 & x \le x_{max} \\ \dfrac{1}{1+\left|\dfrac{x - x_{max}}{x_{max}}\right|} & x > x_{max} \end{cases} \quad (3)$$

A general framework for establishing a design fitness function has now been set forth. The method to obtain the mass, power loss, and the values of c_i for various specifications needed to evaluate the fitness function are detailed below.

A. *Mass and power loss metrics*

In order to evaluate the fitness function, M_{pass}, the total mass of the inductors and capacitors and P_{pass}, the dc power loss in the inductors must be found. These are calculated as the sum of the masses and losses of the individual elements. The mass and dc power loss of the inductors is estimated based on [21] wherein a meta-model is developed for UI core inductors. Current density is used to parametrize the set of Pareto-optimal UI core inductor designs. In particular, the mass and dc power loss in the inductor can be obtained as a function of inductance and current density. The mass of an inductor is obtained as

$$M_{ind} = c_m E_m^* \prod_{k=1}^{K_M} \left(J_{pk} E_M^{*1/3} + b_{M,k} \right)^{n_{M,k}} \quad (4)$$

$$E_m^* = \frac{1}{2} L^* i_{pk}^2 \quad (5)$$

The variable, L^*, is the value of the inductance for which the inductor is designed for, i_{pk} is the peak current at which the inductance is guaranteed to be at least L^* and J_{pk} is the current density corresponding to i_{pk}. The values of the parameters, $b_{M,k}$ and $n_{M,k}$ can be obtained from [21]. Similarly, the dc power loss in the inductors can be obtained as

$$P_{ind} = c_P E_M^{*1/3} \prod_{k=1}^{K_P} \left(J_{pk} E_M^{*1/3} + b_{P,k} \right)^{n_{P,k}} \quad (6)$$

The mass of the capacitors have been obtained by using a curve fit of a set of commercially available capacitors based on the rated voltage. Fifty-four commercially available polypropylene based capacitors were chosen from leading manufacturers based on a voltage rating of 1000 V to 1100 V. A linear fit was sufficient to adequately represent the capacitances as seen in Fig. 3. Thus,

$$M_{cap} = g_1 + g_2 C \quad (7)$$

where C is the value of the capacitance and g_1 and g_2 are constants obtained from the curve fit. The constant g_1 is equal to 0.1977 kg and the constant g_2 is equal to 2.0628·103 kg/F. Another approach wherein the mass of the capacitor is obtained as a function of its rating is presented in [29]. Note that the capacitor metamodel is a function of the voltage requirements.

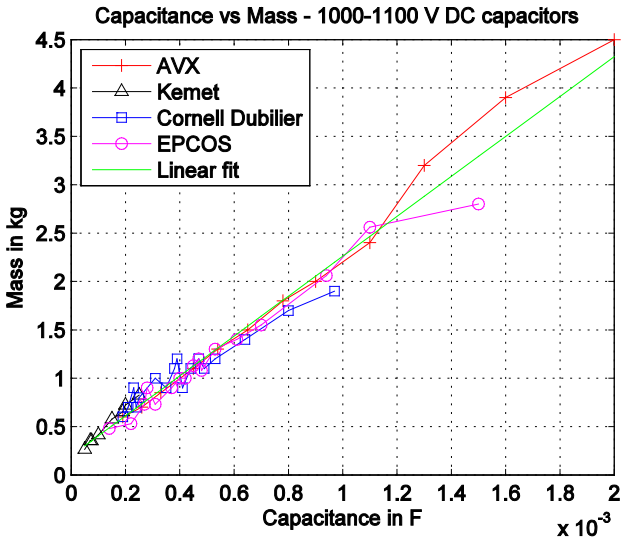

Fig. 3. Linear fit for capacitor mass

B. *Transient specifications*

The time domain behavior of the dc bus voltage during transient events such as load changes and faults are of interest. An example of time-domain specifications for a 28 V dc system and for a 270 V dc system for military aircraft are presented in [22]. A similar approach is suggested in this work, wherein the time domain bus voltage waveforms need to stay within specified envelops during system events. The shape and parameters that characterize these envelopes are shown in Fig. 4.

Now, consider the situation shown in Fig. 4c. The bus voltage (shown as the orange trace) during an event is seen to violate the bus envelope. The constraint is then formulated as

$$c_{i,td} = \begin{cases} \dfrac{1}{1+\mathrm{rms}(v_{viol})} & \text{if constraint violated for } t_{event} < t < t_{endc} \\ 1 & \text{if constraint satisfied} \\ 0 & \text{if constraint not evaluated} \end{cases} \quad (8)$$

where v_{viol} is the part of the bus voltage waveform that has violated the constraint, t_{event} is the time of event, and t_{endc} is

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the time when the check for that particular constraint ends. Thus, if the constraint is never violated during that time, then c_i is one. If it is violated, then the closer the bus voltage is to satisfying the transient event constraint the closer c_i gets to 1. The time-domain average value model of the complete dc power distribution system, which captures the non-linear dynamics of the system in an average value sense, is used to obtain the dc bus voltages time-domain waveforms over a range of set-points, load changes and a line-to-line fault. Thus, the time-domain simulation information is required for the purpose of evaluating whether the design candidate satisfies the transient requirements. To achieve this, a simulation model of the system, which is computationally tractable and sufficiently accurate needs to be used. Non-linear average value models, which capture the non-linear dynamics without the need to simulate power electronic switching behavior are ideal for this kind of analysis.

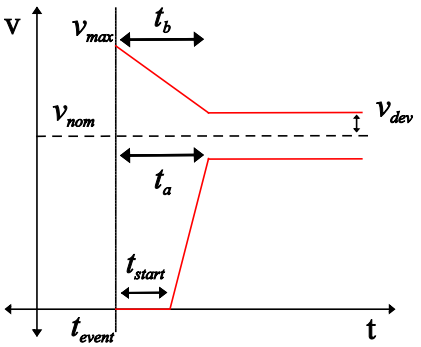

Fig. 4a. Start-up envelope

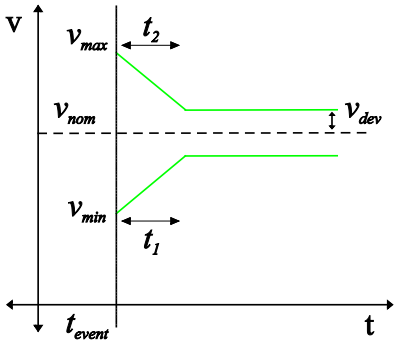

Fig. 4b. Transient event envelope

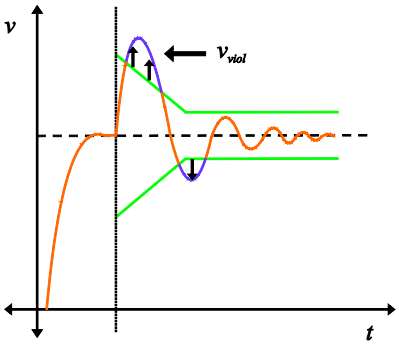

Fig. 4c. Bus voltage with envelope

C. *Distortion specifications*

The power electronics in the system components create distortion or ripple in the dc waveforms due to their switching behavior. This distortion has to be limited to acceptable levels to ensure proper system operation. Distortion will be considered a system component level specification – meaning, the distortion in steady state with typical loads for each system component will be used as a measure for distortion. A distortion model is developed for each system component that can provide this information given the system parameters. Let $\overline{\Delta x_i}$ represent the steady state rms distortion of a current or voltage at the bus, and r_i denote the percentage rms distortion allowed divided by 100. Finally, let x_i^* denote the steady state voltage or current at full load. Then the distortion constraint is formulated as

$$c_{i,dist} = \text{lte}(\overline{\Delta x_i}, r_i x_i^*) \tag{9}$$

where the function lte() is defined in (3). Detailed distortion models for the system are set forth in [27]. Depending upon the component, these are based either on an analytical solution for the voltage ripple, or on a reduced-scope time domain simulation. The key aspect of this formulation is that the constraint value will be one if the rms distortion $\overline{\Delta x_i}$ is less than the allowed distortion $r_i x_i^*$, but less than one if not. If the value is less than one, the average constraint c_{avg} will be less than 1, the elements of the fitness vector will be negative, and the design will be considered non-viable.

D. *Stability and eigenvalue specifications*

Power electronics converters provide excellent load regulation. However, this can lead to a phenomenon known as negative impedance instability [30]. This can result in low-frequency oscillatory behavior in the bus voltages that can eventually lead to system failure. The ability to predict and prevent this type of instability during the design stage leads to a more robust system.

In this work, stability is addressed as a constraint. The first stability check deals with the eigenvalue placement for each system component. Physically, this stability check is aimed at the requirement that each source component can operate in a stable fashion when supplying an ideal (constant current) load, and that each load can operate in a stable fashion when supplied from an ideal (constant voltage) source. It corresponds to a requirement of open loop stability of each component. This is not strictly speaking necessary, but is physically desirable and significantly simplifies the stability analysis since it precludes the existence of open-loop poles in the right-half plane.

The linear model of each system component is obtained at operating points spanning the working range of operation. Since the eigenvalues cannot be obtained at each and every operating point, an approximation is made wherein the range of operation is divided into a fixed number of operating points. The eigenvalues are then obtained at these operating points.

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Consider the s-plane shown in Fig. 5. Typically, the linear system is considered asymptotically stable if all the eigenvalues lie on the left half-plane. However, sometimes, due to parameter uncertainties, it is possible that some eigenvalues may lie very close to the imaginary axis for some designs. To prevent this another boundary for the eigenvalues is proposed which starts at the origin and moves into the left half-plane at an angle ϕ to the imaginary axis. This can also be thought of as a minimum damping factor requirement. Let n_{eig} denote the number of eigenvalues and n_{op} denote the number of operating points. Then, a total of $n_{op} \bullet n_{eig}$ operating points are obtained. A length $l_{j,k}$ where j stands for the j^{th} eigenvalue and k stands for the k^{th} operating point is defined as

$$l_{j,k} = \begin{cases} 0 & \text{if the eigenvalue is to the left of line} \\ l & \text{if the eigenvalue is to the right of line} \end{cases} \quad (10)$$

where l is the real axis distance of the eigenvalue from the dotted line, when it lies to the right of it. The eigenvalue constraint can now be evaluated as

$$c_{i,eig} = \frac{1}{1+\sum_{k=1}^{n_{op}}\sum_{j=1}^{n_{eig}} l_{j,k}} \quad (11)$$

This construction is such that if all the eigenvalues are in the acceptable region, the constraint variable is 1. Otherwise, as eigenvalues move into the unacceptable region, the constraint decreases, causing the average constraint cavg to be less than one, in turn causing the fitness to be negative.

Generalized immittance based stability analysis [24] is an established method to determine the stability of interconnected system components in a dc power distribution system, which is based on the Nyquist stability criterion. A detailed development of this concept can be seen in references [31-34] as well. The immittance (impedance or admittance) over a range of operating points is represented by a closed, convex set of points that encloses the individual immittances at each frequency of interest. This set of points is known as the generalized immittance. Using a series of network reductions, some of which are subject to stability sub-tests [31], the stability problem reduces to a single source-single load stability problem. The stability of the reduced system can then be finally determined by comparing the load admittance to a forbidden region which is based on a desired stability criterion and the source impedance. If this test and all the sub-tests are passed, then the system satisfies stability requirements for all operating points in the domain of interest. Thus, using generalized immittance based stability analysis, the stability constraint can be obtained as

$$c_{i,stab} = \begin{cases} 0 & \text{not all tests satisfied} \\ 1 & \text{all tests satisfied} \end{cases} \quad (12)$$

A highly detailed discussion of these points is set forth in [27].

At this point, all the specifications have been cast at constraints or metrics which come together to form a fitness function which is maximized using an optimization engine. In theory any multi-objective optimization engine could be used. For this work we have chosen to use a genetic algorithm [35, 36] since the problem objective function is not continuous and not convex. While experience is proven that this is certainly a viable method, other methods may work as well or better.

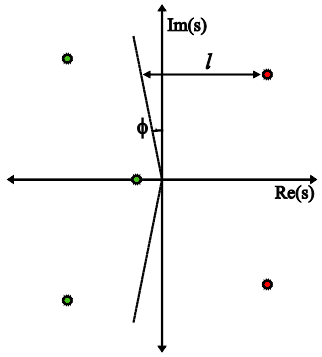

Fig. 5. Eigenvalue constraint

III. REPRESENTATIVE DC DISTRIBUTION SYSTEM

To demonstrate the proposed design methodology, a representative dc power distribution is considered. This power distribution system, shown in Fig. 6, consists of a generation system (GS) connected to two parallel branches. Each branch consists of a dc-dc converter module (CM) and a buck converter based constant power load (CPL). Various models are developed for each of these system component and these are used in the complete system design. A short description of each system component is provided in the sections below. Various models of the system components listed below have been developed and a detailed individual analysis is provided in [27].

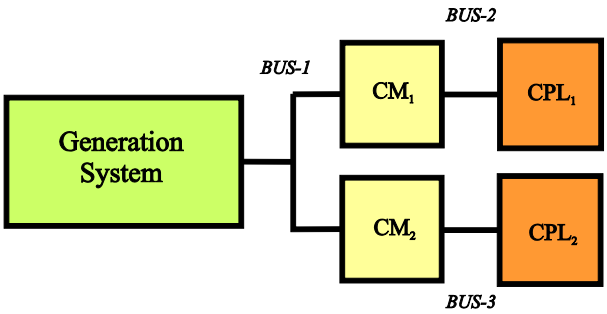

Fig. 6. Representative DC power distribution system

A. Generation System

The generation system (GS) used in this work is a permanent magnet synchronous machine (PMSM) based generator connected to an active rectifier which is controlled by the voltage regulator (VR). It is rated to supply 25 kW and prime mover (PM) shaft spins at 3600 rpm. The dc link voltage is regulated to be 750 V at BUS-1 in Fig. 6. The schematic of the generation system is shown in Fig. 7. It consists of a PMSM acting as a synchronous generator (SG) driven by a prime mover, a hysteresis current controlled three phase bridge inverter which acts as an active rectifier, and an output LC low-pass filter.

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The control diagram is shown in Fig. 8. Herein v_{dc}^{**} is the commanded voltage at the output filter capacitor, v_{dc} is the voltage across the output filter capacitor and i_{mv} is the output filter inductor current. The low-pass filtered values of v_{dc} and i_{mv} are denoted by v_{dclpf} and i_{mvlpf} respectively. The slew-rate limited voltage command is denoted by v_{dc}^{*} . The droop is added to facilitate load sharing, but since only one generation system is used, the droop constant, k_d , is set to zero. In the generation system, the PI control gains, the anti-windup gain, output filter passive component values and the peak load current density of the filter inductor are the parameters that are chosen by the design method.

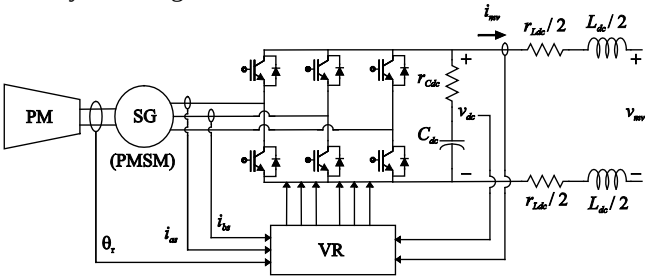

Fig. 7. Generation System

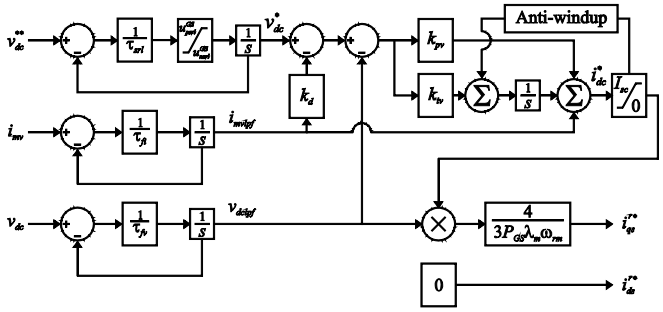

Fig. 8. Control of Generation System

B. Converter Module

Loads in a dc power distribution system are often connected to the distribution bus through dc-dc converters. The choice of topology of the dc-dc converter depends on the application. For shipboard applications, features such as galvanic isolation and effective fault protection are desirable. The topology and the control used in this work is shown in Fig. 9 and Fig. 10. Herein, v^{*} is the commanded output voltage, v_{of} is the output filter capacitor voltage, and i_{pmax} is the peak per cycle transformer primary current. Some salient aspects of this topology are (a) it provides galvanic isolation, (b) LC low pass filters at both the front-end and at the load side reduce distortion propagated to the source, and (c) the peak current control provides appropriate protection to the active devices and prevents fault propagation to the generation side. The average value modeling of the converter and the control can be found in [37]. The switching frequency of the converter module is assumed to be 20 kHz. In the converter module, the PI control gains, the anti-windup gain, the LC input and output filter passive component values, the rectifier inductor value, and the peak load current density of the inductors are the parameters that are chosen by the design method.

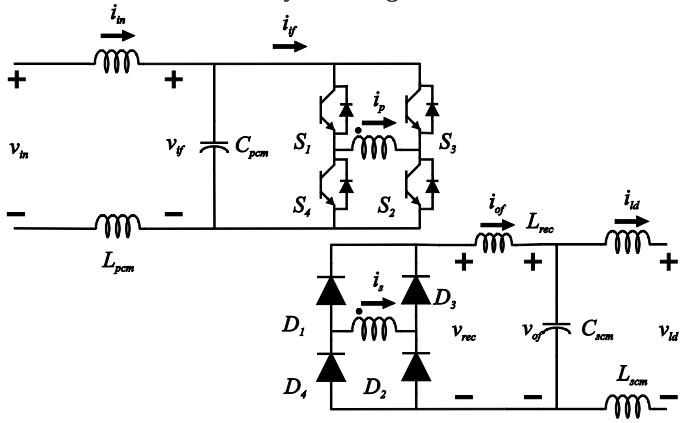

Fig. 9. Converter module

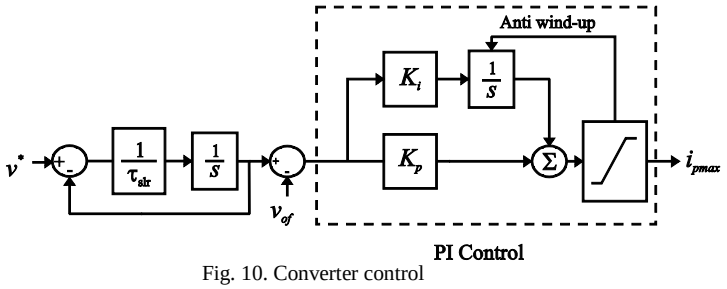

Fig. 10. Converter control

C. Buck Converter based Constant Power Load

A constant power load can be defined as a load that consumes constant power from a source for a working range of dc bus voltages [38]. The rapid proliferation of power electronics has led to many system components which behave as constant power loads. For example, a tightly regulated motor drive supplying constant torque behaves as a constant power load [30]. In [39], a characterization of various types of constant power loads on an aircraft power supply system is described. It has been noted that most of the constant power loads on a dc power distribution system on the aircraft are tightly regulated dc-dc converters. The buck converter based constant power load used in this work and the control used are shown in Fig. 11 and Fig. 12 respectively. Herein, v_b and v_b^{*} are the buck converter output filter voltage and the voltage command, P^{*} is the constant power drawn and v_{Ccpl} is the input filter capacitor voltage. The output voltage of the buck converter is regulated by a PI controller with non-linear

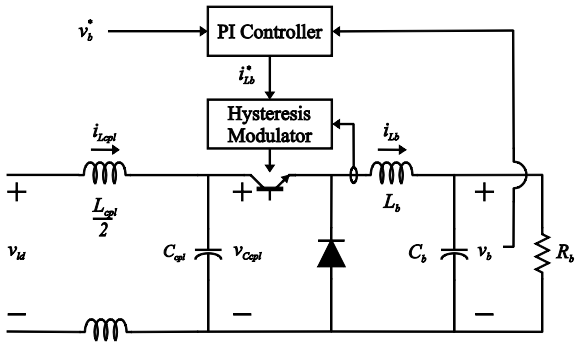

Fig. 11. Buck converter based constant power load

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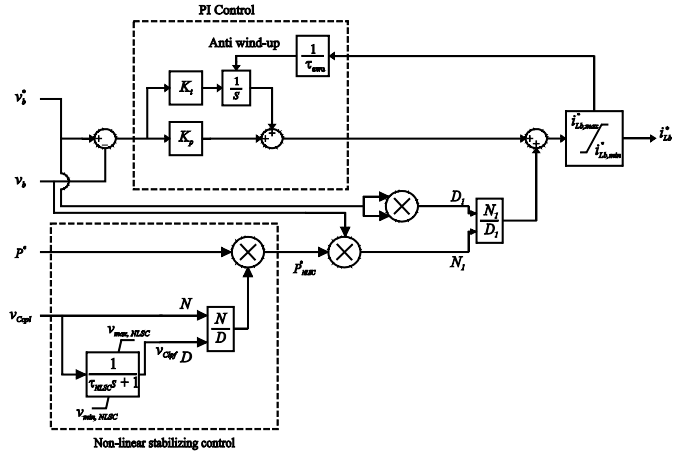

Fig. 12. Control of buck converter with non-linear stabilizing control

stabilizing control [40] which is a non-linear control strategy aimed at mitigating the negative impedance instability issues caused by constant power loads. In the constant power load, the non-linear stabilizing control gain, the input LC filter passive component values and the peak load current density of the filter inductor are the parameters that are chosen by the design method.

IV. Case Study

For the representative dc power distribution system shown in Fig. 6 with the various system components described in Section III, the design based on the methodology proposed in Section II will be presented here. The first step is to define the design space. The design space consists of parameters that need to be chosen through the optimization process by the optimization engine such that the fitness function is maximized.

Table I defines the parameters selected for the optimization, as well as the ranges of allowed values. As can be seen very broad ranges were chosen for most parameters in order to see what is selected. In other words, it was desired that the parameter values and control gains be selected by the algorithm, without imposing too much of a pre-conceived idea about what the values would be. The one exception to this would be the inductor current densities. Here the upper limit corresponds to a practical thermal limit for a passively air cooled device, and the lower limit would be considered very low in practice. The appropriateness of the limit will be ascertained from a parameter distribution plot which will be discussed later in this section.

The next step is to define the various constraints as described in Section II. A set of events need to be defined to evaluate the time-domain transient system performance. Events such as full load start-up at rated voltage, 90% load drop and increase at various dc bus voltages, a bolted line-to-line fault on one of the converters, etc. have been used. The rated BUS-1 voltage is 750 V, BUS-2 and BUS-3 voltages are 400V. The system should be able to operate satisfactorily within a working range of the rated voltage. It is assumed in this work that a set-point deviation of ±50 V is acceptable. Thus, the following operating conditions have been used for $\{v_{bus1}, v_{bus2}, v_{bus3}\}$ in the time-domain simulations: (a) {700V, 350V, 400V}, (b) {700 V, 450 V, 400V}, (c) {800 V, 350 V, 400 V}, (d) {800 V, 450 V, 400 V}. A bolted line-to-line fault has also been simulated on BUS-2 to ensure that even if there is a fault in one leg of the system, the other leg operates without issues. Clearly this does not cover the entire gamut of operating points. However, ensuring that the system behavior is acceptable under extreme conditions can give reasonable confidence about system behavior under normal operation. The set of events used in the transient simulation are given in Table II. The various parameters defining the start-up and transient event envelopes also need to be set. These are defined in Table III and Table IV respectively.

Table I. Design space

Gene	Parameter	Min	Max
1	Proportional gain - GS	1e-3 Ω^{-1}	1e3 Ω^{-1}
2	Integral gain - GS	1e-3$(\Omega s)^{-1}$	1e3 $(\Omega s)^{-1}$
3	Anti-windup constant - GS	1e-3 s	1e-1 s
4	Proportional gain - CM	1e-3 Ω^{-1}	1e3 Ω^{-1}
5	Integral gain - CM	1e-3 $(\Omega s)^{-1}$	1e3 $(\Omega s)^{-1}$
6	Anti-windup constant - CM	1e-3 s	1e-1 s
7	Non-linear stabilizing constant - CPL	1e-3 s	1e-1 s
8	DC output capacitance – GS	1e-4 F	1e-1 F
9	Input filter capacitance - CM	1e-4 F	1e-1 F
10	Output filter capacitance – CM	1e-4 F	1e-1 F
11	Input filter capacitance – CPL	1e-4 F	1e-1 F
12	DC output inductance – GS	1e-5 H	1e-1 H
13	Input filter inductance – CM	1e-5 H	1e-1 H
14	Output filter inductance - CM	1e-5 H	1e-1 H
15	Rectifier inductance – CM	1e-5 H	1e-1 H
16	Input filter inductance – CPL	1e-5 H	1e-1 H
17	Inductor current density – GS	1e6 Am^{-2}	10e6 Am^{-2}
18	Input filter ind. current density – CM	1e6 Am^{-2}	10e6 Am^{-2}
19	Output filter ind. current density – CM	1e6 Am^{-2}	10e6 Am^{-2}
20	Rectifier ind. current density – CM	1e6 Am^{-2}	10e6 Am^{-2}
21	Input filter ind. current density - CPL	1e6 Am^{-2}	10e6 Am^{-2}

Table I. Events used in design simulation

Event	Time	Event description
1	0 s	Generation system is turned on and a voltage of 750 V is commanded at BUS-1
2	0.6 s	CM-1 and CM-2 are enabled and a voltage to 400 V commanded at BUS-2 and BUS-3
3	1.0 s	CPL-1 and CPL-2 are enabled, each drawing their full-load capacity of 10 kW each
4	1.2 s	700 V commanded at BUS-1, 450 V commanded at BUS-3
5	1.3 s	Step change in CPL-2 load 10% of full load. CPL2 only draws 1 kW at this point
6	1.5 s	CPL-2 brought back up to full load drawing 10 kW
7	1.7 s	350 V is commanded at BUS-3
8	1.8 s	Step change in CPL-2 load to 10% of full load
9	2.0s	CPL-2 brought back up to full load drawing 10 kW
10	2.2 s	800 V is commanded at BUS-1
11	2.4 s	Step change in CPL-2 load to 10% of full load
12	2.6 s	CPL-2 brought back up to full load drawing 10 kW
13	2.8 s	450 V is commanded at BUS-3
14	2.9 s	Step change in CPL-2 load to 10% of full load
15	3.1 s	CPL-2 brought back up to full load drawing 10 kW
16	3.3 s	400 V is commanded at BUS-3
17	3.4 s	Bolted line-to-line fault at BUS-3
18	3.6 s	End of simulation

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In Table III, the start-up constraint envelopes' parameterized values are given. The parameters are defined as described in Fig. 4a, wherein v_{com} is the commanded voltage, v_{dev} is the voltage deviation allowed at steady operation from v_{nom}, t_a and t_b are the times for the lower and upper envelopes to converge to v_{nom} - v_{dev} and v_{nom} + v_{dev} respectively. Similarly in Table IV, the transient constraint parameters are defined as described in Figure 4b.

Table III. Start up transient constraints

Bus	Time(s)	ta(s)	tb(s)	t_{start} (s)	v_{max}(V)	v_{com}(V)	v_{dev}(V)
1	0	0.55	0.6	0.4	800	750	35
2	0.6	0.35	0.35	0.25	500	400	20
3	0.6	0.35	0.35	0.5	500	400	20

Table IV. Transient event constraints

Event	Bus	t_1(s)	t_2(s)	v_{max}(V)	v_{min}(V)	v_{com}(V)	v_{dev}(V)
5,6	1	0.1	0.1	750	650	700	35
5,6	2	0.1	0.1	450	350	400	20
5,6	3	0.1	0.1	500	400	450	22.5
8,9	1	0.1	0.1	750	650	700	35
8,9	2	0.1	0.1	450	350	400	20
8,9	3	0.1	0.1	400	300	350	17.5
11,12	1	0.1	0.1	850	750	800	40
11,12	2	0.1	0.1	450	350	400	20
11,12	3	0.1	0.1	400	300	350	17.5
14,15	1	0.1	0.1	850	750	800	40
14,15	2	0.1	0.1	450	350	400	20
14,15	3	0.1	0.1	500	400	450	22.5
17	1	0.1	0.1	800	700	750	37.5
17	2	0.1	0.1	450	350	400	20

The distortion constraints are detailed in Table V. These specifications only apply to the currents and voltages at the input and output low-pass filters that connect to the dc buses. For the stability constraints, the eigenvalue constraint detailed in Section II requires that the system component eigenvalues have a damping ratio of at least 2.5%. The other parameters that are required for the generalized immittance based stability analysis are detailed in Table VI. The DC Stability Toolbox [41] is a MATLAB based toolbox which can be used for this purpose.

Thus, the specifications for design of the representative dc power distribution system has been established. The next step is to perform the design optimization using the genetic optimization tool. Genetic Optimization Systems Engineering Toolbox (GOSET) [36] is a MATLAB based genetic optimization tool which has been used for performing this optimization based design. In the next section, the results of the optimization will be presented, along with the validation.

Table V. Distortion Constraints

Low-pass filter quantities	Steady-state value	Percent rms distortion allowed
v_{dc} - Output filter capacitor voltage	750 V	2%
i_{mv} - Output filter inductor current	35 A	2%
v_{Cpcm} - Input filter capacitor voltage	750 V	2%
i_{in} - Input filter inductor current	17.5 A	2%
i_{of} - DC link inductor current	30 A	5%
v_{Cscm} - Output filter capacitor voltage	400 V	2%
i_{ld} - Output filter inductor current	30 A	2%
i_{Lcpl} - Output filter capacitor current	30 A	2%
v_{Ccpl} - Output filter capacitor voltage	400 V	2%

Table VI. Stability analysis parameters

s-vector calculation parameters	
Minimum frequency	0.01 Hz
Maximum frequency	10 kHz
Number of frequencies	60
Generalized impedances	
Number of sides	6
Number of intermediate points	3
ESAC stability criterion parameters	
Gain margin	3 db
Phase margin	30 degrees
Truncation radius	60 dB
Points on horizontal line	15
Points on vertical line	5

In order to evaluate the fitness function for a given design candidate, note that all the analyses listed in Section II need to be performed. This include running a time-domain simulation, a distortion calculation, an eigenvalue analysis and a stability evaluation. Since a genetic algorithm based approach is used in this work, the fitness function needs to be evaluated thousands of times. The computational burden increases as the system complexity and the number of system components increases. This is an inherent disadvantage of using this approach. However, with the availability of extremely powerful computational resources and the use of techniques such as parallel processing (which is extremely suitable for genetic algorithm based optimization), these challenges can be met. The design optimization routines evaluated in this work take approximately 5 days per optimization run on an Intel Xeon 8 core 3.4 GHz processer machine with 32 GB of random access memory (RAM). Parallel processing was also used on a single machine (utilizing the multiple cores available) to reduce the computational time.

V. DESIGN OPTIMIZATION RESULTS

The results of the design optimization of the representative dc power distribution system are presented in this section. The optimization routine is executed multiple times to ensure that the results obtained are consistent. A design is selected from the Pareto-optimal front and then validated using a detailed waveform-level simulation.

The Pareto-optimal fronts from four design runs are shown in Fig. 13. The optimization routines were all run with an initial population of 2000 individuals for 80 generations. As seen in Fig. 13, the Pareto-optimal fronts overlap and are reasonably close together. Each colored dot in the gene distribution in Fig. 14 represents a parameter value of the candidate solutions. Each bin denotes the normalized distribution of parameter values over their respective ranges (21 bins for 21 design parameters). The red dots (dots to the right of the bin) represent those design with a lower mass (first objective) than the blue dots (dots to the left of the bin) The distribution of the dots in each bin is an indication of how sensitive the fitness (first objective in this plot) is to changes in that parameter. It is

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also an indication of whether the range chosen is appropriate. If too restrictive a range is chosen, the dots will tend to be arranged close to the maximum or minimum value. As seen in Fig. 14, the spread of the dots is in-between the maximum and minimum values. The gene distributions for the other optimization runs are similar. The Pareto-optimal front of optimization run 4 is shown in Fig. 15. One chosen design candidate is highlighted as a red star. This design will be validated using the waveform-level model. The dc power loss in the passives in this design is 35.8 W and the mass is 63.61 kg. The parameters obtained from the optimization run for this design candidate is shown in Table VII.

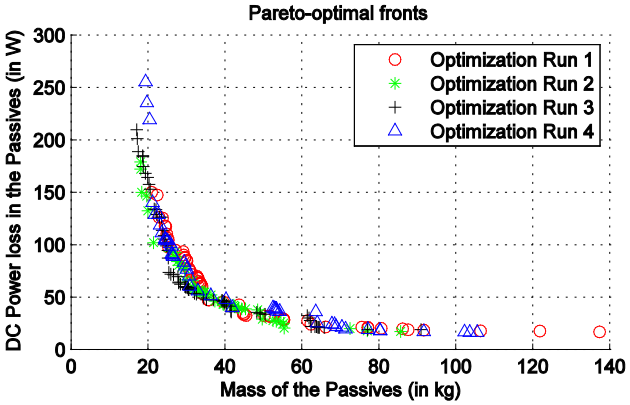

Fig. 13. Pareto-optimal fronts from four optimization runs

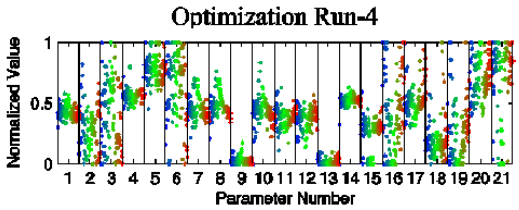

Fig. 14. Gene distribution plot for optimization run - 4

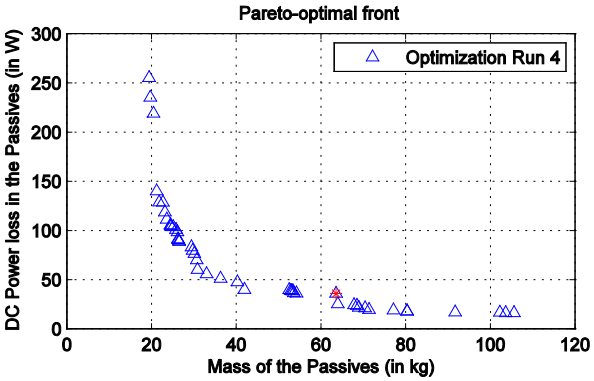

Fig. 15. Optimization run - 4 and the chosen design candidate

Table VII. Chosen design candidate parameters

Gene	Parameter	Value
1	Proportional gain - GS	1.588 Ω
2	Integral gain - GS	0.013 Ωs^{-1}
3	Anti-windup constant - GS	0.078 s
4	Proportional gain - CM	1.174 Ω
5	Integral gain - CM	43.138 Ωs^{-1}
6	Anti-windup constant - CM	0.053 s
7	Non-linear stabilizing constant - CPL	0.001 s
8	DC output capacitance – GS	5.165 mF
9	Input filter capacitance - CM	5.615 mF
10	Output filter capacitance – CM	181.99 µF
11	Input filter capacitance – CPL	3.092 µF
12	DC output inductance – GS	317.8 µH
13	Input filter inductance – CM	46.442 µH
14	Output filter inductance - CM	10.632 µH
15	Rectifier inductance – CM	1.662 mH
16	Input filter inductance – CPL	10.00 µH
17	Inductor current density – GS	1.02e6 A/m^2
18	Input filter ind. current density – CM	4.90e6 A/m^2
19	Output filter ind. current density – CM	2.46e6 A/m^2
20	Rectifier ind. current density – CM	1.82e6 A/m^2
21	Input filter ind. current density - CPL	8.68e6 A/m^2

In this case study, the selection of a particular design from the Pareto-optimal front was arbitrary. However, this selection can also be performed much more systematically. In particular, the Pareto-optimal front shows the trade-off between differential loss and differential mass of the systems (i.e. the portions of mass and loss that will be different between different designs). This trade-off can be ideally used in a higher level system optimization, for example, in a full vehicle optimization wherein the power system is only one part.

The dc bus voltages as obtained from both the average value model (AVM) and the waveform level model (WLM) simulated with the parameters in Table VII are seen in Figures 16, 17 and 18. As seen, the bus voltage remains within the specified start-up and transient envelope for the set of events specified in Table II. The AVM and WLM waveforms also match well.

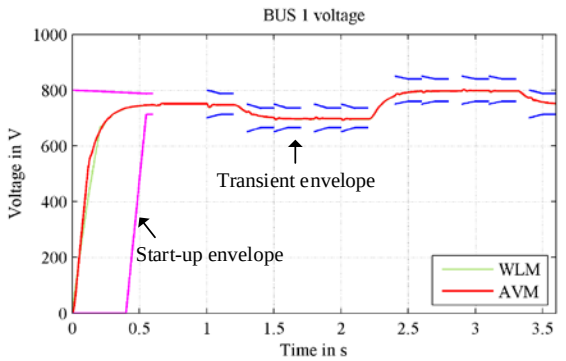

Fig. 16. Bus-1 voltage

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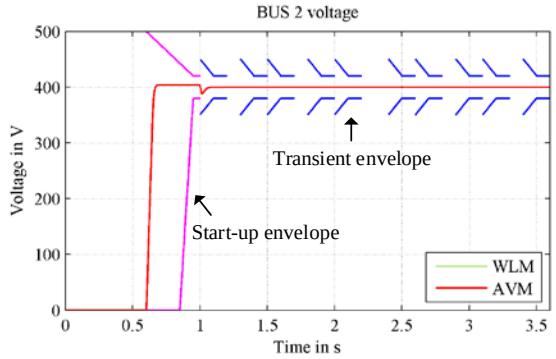

Fig. 17. Bus-2 voltage

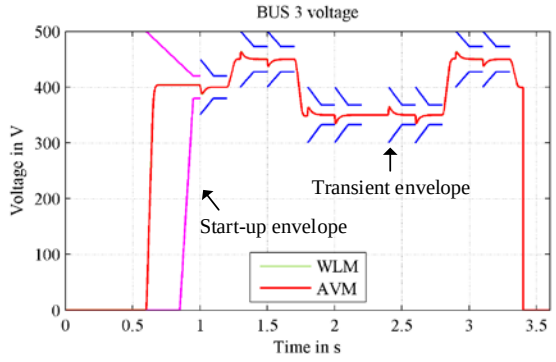

Fig. 18. Bus-3 voltage

The results in Fig. 16-18 demonstrate that the time-domain performance metrics were satisfied for the specified studies. However, the goal is that the system is always well behaved. In order to explore this an alternate set of events as specified in Table VIII are also simulated to verify system behavior. The aim of running this study is to gain further confidence that the chosen design candidate satisfies the requirements not only for the training set of events, but also for other transient events. Both the waveform level model (WLM) and the average value model (AVM) are evaluated for this non-training set of events. As seen in Fig. 19 to Fig. 21, the bus voltages for this scenario also satisfy the start-up and transient specifications.

Next, a visualization of the stability analysis using the generalized immittance based stability analysis method is shown Fig. 22-23 The axis of the figures are the magnitude of admittance, phase of admittance, and frequency. The figures show component admittance versus frequency, as well as a forbidden region of admittance. Stability is garanteed provided the admittance does not intersect the forbidden region. Note that the admittance for a given component is a bounded set of values rather than a single value. The bounded set represents the variation of component admittance due to change of operating conditions or parameters. A complete analysis and explanation of this method is presented in [24].

Table VIII. Non-training set of events

Event	Time	Event description
1	0 s	Generation system is turned on and a voltage of 750 V is commanded at the filter capacitor connected to BUS-1
2	0.6 s	CM-1 and CM-2 are enabled and a voltage to 400 V is commanded at the output filter capacitor connected to BUS-2 and BUS-3
3	1.0 s	CPL-1 and CPL-2 are enabled, each drawing their full-load capacity of 10 kW each
4	1.2 s	Step change in CPL-2 load 10% of full load. CPL2 only draws 1 kW at this point
5	1.4 s	Step change in CPL-1 load 10% of full load. CPL1 only draws 1 kW at this point
7	1.6 s	Both CPL-1 and CPL-2 brought back up to full load drawing 10 kW each
8	1.8 s	End of simulation

In this method, the immittance (impedance or admittance) is obtained for each system component over a range of operating points. The system is then reduced based on methods detailed in [27] to a source-load system at each bus. Consider the equivalent source-load system at Bus-1. The impedance of the generation system is used to obtain a admittance constraint which is a forbidden region for the equivalent load (which consists of the two branches), based on the Nyquist stability criterion. This can be visualized using 3-D plots to ensure that the generalized impedance/admittance does not intersect with the forbidden region. In Fig. 22 and Fig. 23, the forbidden region for the admittance of the source and the admittance of the load is presented. If there is no intersection between these regions then, the stability specification has been satisfied. As seen in Fig. 22 and Fig. 23, there is no intersection seen for the chosen design candidate, as is expected.

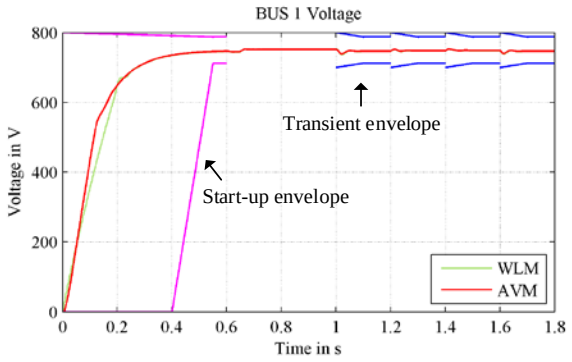

Fig. 19. Non-training set of events – Voltage at Bus-1

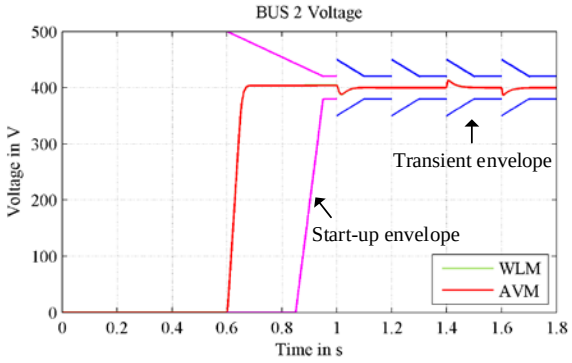

Fig. 20. Non-training set of events – Voltage at Bus-2

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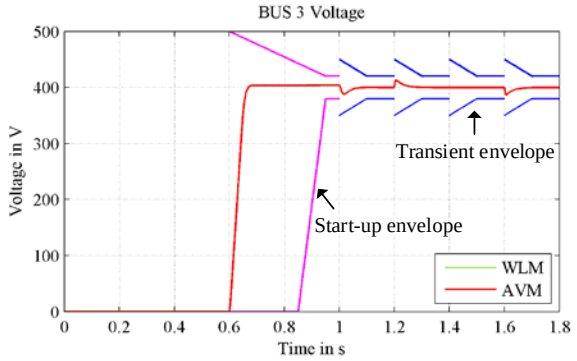

Fig. 21. Non-training set of events – Voltage at Bus-3

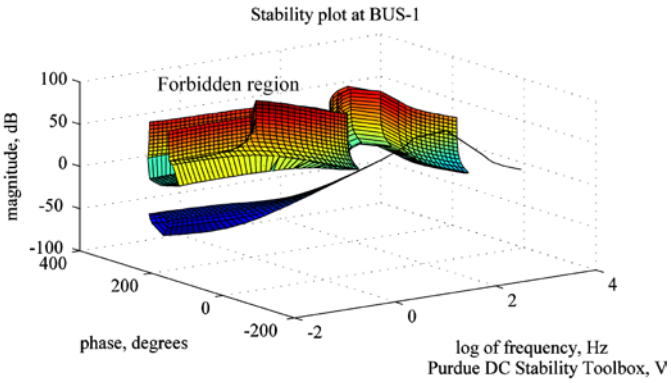

Fig. 22. Admittance space plot of GS- (CM1,CM2) interface (Admittance constraint obtained from GS impedance and the effective load admittance obtained by combining CM1 and CM admittances)

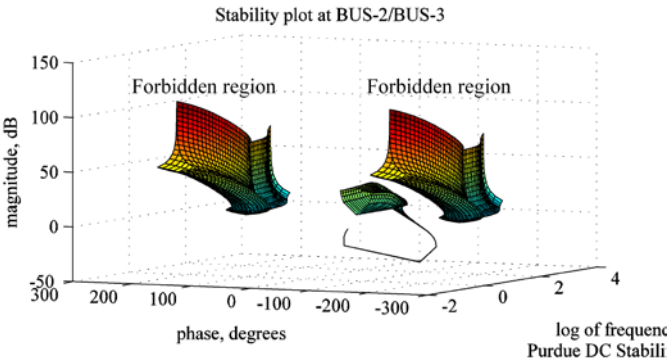

Fig. 23 Admittance space plot of CM-CPL interface (Admittance constraint obtained from effective CM output impedance and load admittance obtained from CPL)

VI. SUMMARY AND FUTURE WORK

A large body of literature exists wherein the individual system components such as dc-dc converters or a generator with a rectifier front end are designed in detail. Though the focus of these works is the design of each of these components, there is a gap in literature wherein the interaction between various system components is captured in the design process. The disadvantage of needing to be overly conservative in the design of individual system components when designing them separately is avoided by following this approach.

The central idea of this work is to pose the design problem as an optimization problem wherein time-domain analysis, distortion analysis, stability analysis, mass, and loss are simultaneously considered in choosing the control gains and passive components of a dc power distribution system. Transient requirements are evaluated using a time-domain average value model, power quality requirements are evaluated using a distortion model, and stability analysis is utilized to ensure that issues such as negative impedance instability are avoided at the design stage itself. Also, the design process is streamlined and repetitive design steps are avoided, saving valuable design time for the system designer. One of the disadvantages of using this approach is that it is computationally intensive. As the size of the system increases, the computational burden increases as well. However, computation time is insignificant compared with the savings in engineering time.

In this work, an inductor meta-model is used to obtain the inductor mass and dc power losses. Only UI core inductors are considered in the meta-model formulation. Expanding the meta-model formulation to other common inductor topologies can increase the scope for optimization. Development of meta-models for transformers and other components such as electric machines can provide a more comprehensive solution for the design of dc power distribution system in the same vein as this work. This work could also be advanced by including switching frequency as a design parameter. Recall that in the study conducted such far it was assumed that the switching frequency is chosen to be the maximum recommended value for the given semiconductor. The switching and conduction losses in the converter module and losses in the passives will change with a change in switching frequency, as will the distortion. Thus, allowing the switching frequency to be selected by the design algorithm may lead to improved designs (or may simply lead to the selection of the maximum allowed frequency). Another feature that would lead to improved design would be by increasing time domain model fidelity – for example by including control latency.

It should be noted that while the proposed approach is focused on systems in which the system is not regularly reconfigured by the addition of new components, it may be extended to such a circumstance. In such a case, a redesign is conducted with the addition of the new component but the degrees of freedom are limited to quantities associated with that new component. In this case, the redesign focuses on the best incremental change rather than the best overall system performance.

ACKNOWLEDGMENT

The authors would like to acknowledge the support of the Office of Naval Research Grant N000141410160 and ABB Inc. .

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