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A Fully Differential CMOS Current Memory Cell for Space-Embedded Analog-to-Digital Converters

Olivier Bernal, *Member, IEEE*, Marc Cousineau, *Member, IEEE*, and Marc Lescure

***Abstract*—This paper presents a radiation-hardened high-resolution current memory cell (CMC) that can be used to implement *current-mode* analog-to-digital converters (ADCs) for space-embedded, charge-coupled device processors. This CMC is based on a fully differential structure and on the Miller effect to reduce charge-injection errors. Using a commercial 0.35-μm 3.3-V complementary metal–oxide–semiconductor (CMOS) process, the radiation tolerance of this CMC has been enhanced by designing enclosed n-channel MOS transistors, using p-channel MOS switches only, and introducing guard rings wherever necessary. Results show that the CMC accuracy is 10 bits and that its estimated linearity error is $\pm$50 nA for a [$-$200 μA; 200 μA] dynamic input current range. Experimental results point out that signal-dependent charge injections are divided 23 times at least, which improves the CMC accuracy by approximately 4 bits. The measured acquisition time for a 200-μA input step transition to achieve a 10-bit settling accuracy is 50 ns. The active chip area and the power consumption of the proposed CMC are 0.042 mm^2 and 6 mW, respectively.**

***Index Terms*—Charge-coupled device (CCD) processors, complementary metal–oxide–semiconductor (CMOS), current memory cell (CMC), current-pipelined analog-to-digital converter (ADC), low power, low voltage, Miller effect, space-embedded system.**

I. Introduction

OVER THE LAST few years, circuit technologies used in space-embedded systems have evolved from radiation-hardened (rad-hard) technologies to more conventional complementary metal–oxide–semiconductor (CMOS)/Bipolar CMOS (BiCMOS) technologies for three main reasons: 1) less cost; 2) easier access to these technologies; and 3) greater integration. Full monolithic CMOS analog front ends (AFEs) are required for low-power consumption and higher level integration purposes. Moreover, to obtain high-resolution images, analog-to-digital converters (ADCs) used in AFEs [or in charge-coupled device (CCD) processors] must achieve sampling rates of more than 10 MS/s with a linearity in the range of 10–14 bits. Even if 10- to 16-bit resolution at 10–60 MS/s is achieved by standard commercial AFEs, they have not been designed to withstand space environment conditions. Indeed, extra special design and layout considerations are needed for MOS device and circuit radiation-hardening purposes.

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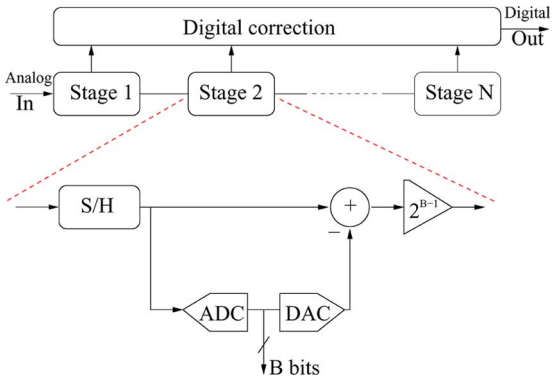

Fig. 1. Block diagram of a pipelined ADC.

There is a wide variety of ADC architectures. Each has its strengths and weaknesses that make it appropriate for a given set of specifications, such as speed, resolution, and power. Among all architectures, pipelined ADCs suit previous performances (see Fig. 1). Furthermore, pipelined ADC accuracy relies on the resolution of the first stages, which means that first-stage design should be taken care of.

In this paper, instead of *voltage-mode* circuits, *current-mode* circuits have been chosen for their low-power/low-voltage characteristics and for their extended dynamic input ranges. Dynamic current mirrors [1], which are also known as current memory cells (CMCs), have been studied as an alternative for designing accurate ADCs [2] and filters. The CMC is equivalent to a sample-and-hold circuit in *voltage-mode* circuits. Fig. 2 shows how such a CMC can be implemented within a current-pipelined ADC [2], [3]. Although switched-current circuit accuracy is mainly limited by charge-injection errors induced by switches [4] and by the finite output conductance of current sources, CMC can achieve high-linearity [5] and high-sampling-rate [6] performances.

The aim of this paper is to present a rad-hard fully differential CMC that achieves 10-bit accuracy and an estimated $\pm$50-nA nonlinearity error at 10 MS/s while dissipating only 6 mW in a 0.35-μm, 3.3-V CMOS process.

II. CMC Principle

A CMC can be achieved within a single transistor T_m (Fig. 3). It operates on a two-phase basis. During the first phase

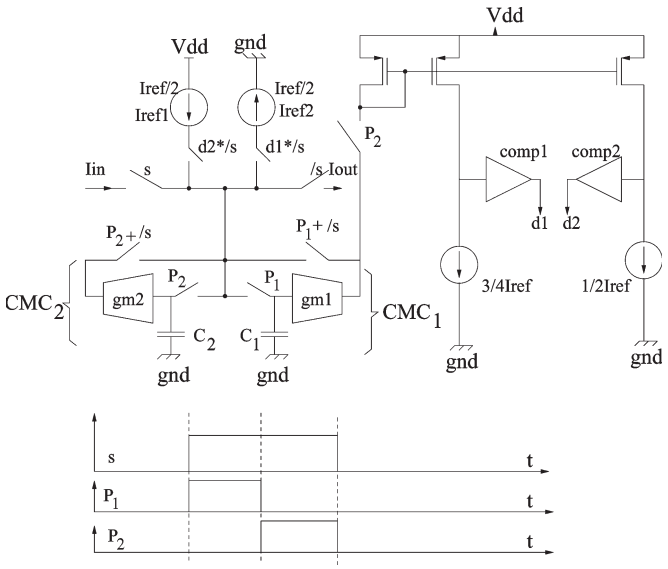

Fig. 2. Schematic diagram of one current-pipelined ADC stage (single-ended version).

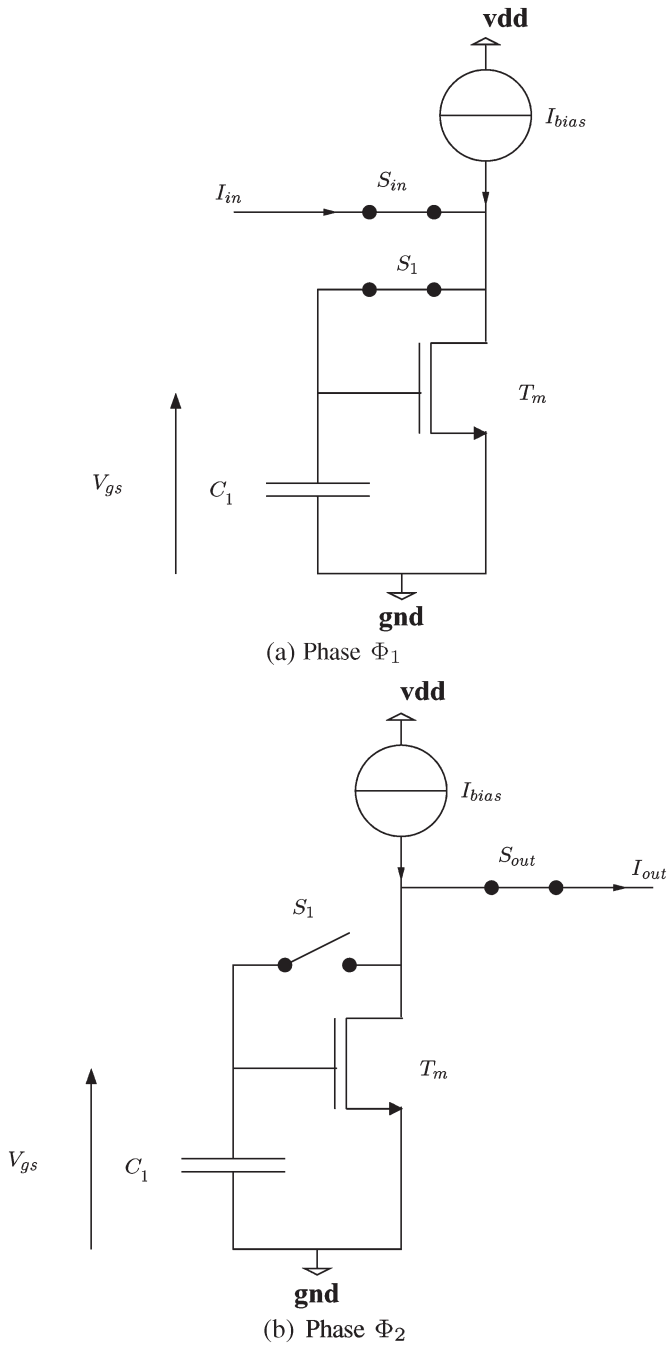

Fig. 3. Basic CMC. (a) Sampling phase (b) Holding phase.

[sampling phase Fig. 3(a)], switches S_1 and $S_{\rm in}$ are closed. It allows current $I_{\rm in} + I_{\rm bias}$ to flow through T_m. Then, during the second phase [holding phase in Fig. 3(b)], by opening S_1, the value of V_{gs} at the end of the first phase is held on the holding capacitor C_1, thereby sustaining T_m's current at $I_{\rm in} + I_{\rm bias}$. Finally, $I_{\rm in}$ is transferred to $I_{\rm out} = -I_{\rm in}$ by closing $S_{\rm out}$.

The CMC accuracy is thus mainly limited by three factors: 1) the CMC finite output conductance; 2) capacitive coupling between the drain and gate of T_m; and 3) the charge-injection error induced by S_1.

Regulated cascode techniques can be applied to reduce the current transmission error between CMCs by diminishing the CMC output conductances. Using such structures, CMC output impedances can be approximately 100 times higher than non-cascoded structures [7], [8].

Furthermore, to reduce charge-injection errors, thereby increasing the CMC accuracy, different techniques can be used, such as constant voltage switching methods [9], [10], the Miller effect [2], [10], [11], and dummy switches. In this paper, the Miller effect technique is employed to improve the CMC accuracy with minimum stability penalty.

III. DME-CMC

Fig. 4 depicts a simplified single-ended version of the differential Miller effect CMC (DME-CMC) for better understanding, whereas Fig. 5 presents the fully differential cell with its common-mode feedback (CMFB) circuit. Note that regulated cascode architectures are not shown for simplicity. The fully differential structure has been chosen for two main reasons: First, fully differential architectures allow a higher level of analog performance, because distortion effects are greatly reduced by suppression of even-order harmonics. They also offer better immunity against power line noises, as well as crosstalk from neighboring digital circuits. Second, its fully differential architecture allows one to simplify the whole design of the CMC. There is no longer any need for buffers as in [10], because the structure intrinsically rejects common-mode errors at the cost of a reduced dynamic range. Furthermore, a differential charge-injection error attenuation circuit can be obtained by employing a fully differential Miller feedback circuitry (see Fig. 5) similar to that reported in [10] and [12]. Both the operation of switches at virtual ground and the Miller capacitance effect technique are used to achieve greater performances.

A. Miller Feedback Circuit Description

The different circuit operations involve one sample and one hold mode (refer to Fig. 5). For better understanding of

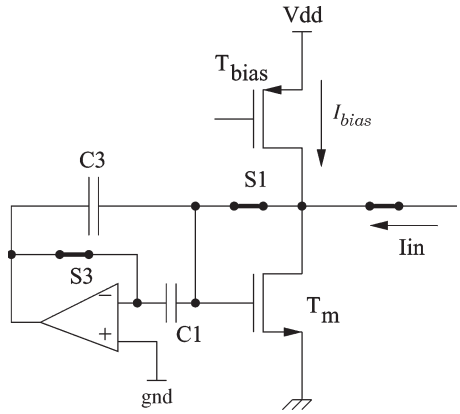

Fig. 4. Simplified single-ended version of the DME-CMC.

circuit operations, Fig. 6(a) and (b) shows the different states of the involved switches during the sampling and holding phases. In the sample mode, all switches, except P_2, are closed. Hence, the operational amplifier (Opamp) of the DME-CMC is self-biased to $V_{\rm cm}$ ($\approx V_{dd}/2$) due to its own CMFB, and the differential input signal current flows through T_1 and T_2. During this phase, the capacitor pair C_1 and C_3 (and also C_2 and C_4) and the transistor gate of T_1 (T_2) are charged to allow a $I_{\rm bias} + I_{\rm in^+}(I_{\rm bias} - I_{\rm in^-})$ current to flow through the drain of T_1 (T_2). Before switching to hold mode, switches S_3 and S_4 are opened to enable the Miller capacitance effect. Since the drain and source of S_3 and S_4 are biased at the same voltage $V_{\rm cm}$ (Opamp common-mode voltage) just before being turned off, the charges injected by S_3 and S_4 into C_1 and C_2 and the input entrances of the Opamp should not only be identical but also input signal independent (mismatches are not taken into account here). As a consequence, this charge injection should appear mainly as a common-mode error, which is rejected by the differential architecture of the CMC. Then, switches S_1 and S_2 can be turned off. Therefore, differential charge-injection errors, which are signal dependent, are reduced by the Miller capacitance effect (note that common charge injection is still rejected by the differential structure). As a consequence, differential error voltage $\Delta V_{\rm inj}$ [10] is given by

$$\Delta V_{\rm inj} \approx \frac{\Delta q}{2C_{\rm Miller}} \quad \text{with} \quad C_{\rm Miller} = \left(1 + \frac{A_d}{2}\right) \cdot C_3 \qquad (1)$$

where A_d is the Opamp open-loop gain, and $\Delta q = \delta q_{S_1} - \delta q_{S_2}$ is the differential injected charges (δq_{S_x} is the injected charges from S_x). Therefore, the Opamp open-loop gain and bandwidth should be carefully chosen to achieve high accuracy. The differential current error is given by [T_1 and T_2 are both assumed to work in the saturation region (strong inversion)]

$$\Delta I_D = \delta I_{D(T_1)} - \delta I_{D(T_2)}.$$

This error can be approximated by [4]

$$\Delta I_D \approx \alpha \frac{C_{\rm ch}}{2C_{\rm Miller}}(1 + \gamma_{\rm body}/3) I_{\rm bias} m \qquad (2)$$

where m is the current modulation [$I_{\rm in_+} = I_{\rm bias}(1+m)$ and $I_{\rm in_-} = I_{\rm bias}(1-m)$]; α is the proportion of switch charges, which are injected into hold capacitors ($0 < \alpha < 1$); $\gamma_{\rm body}$ is the body effect coefficient; and $C_{\rm ch}$ is the total gate capacitance of switch MOS S_1 (S_2) [13].

To achieve 13-bit accuracy for $I_{\rm bias} = 250$ μA and $m = 0.4$, $C_{\rm Miller}$ should be chosen so that $\Delta I_D < 25$ nA ($(1/2)$ LSB). Note, however, that, according to (2), the CMC linearity will be higher. As a consequence, according to (1) and (2), and assuming that $\alpha = 0.5$, the Opamp gain should be greater than 52 dB [p-channel MOS (PMOS) switch size of 20 μm/0.5 μm]. Nevertheless, the DME-CMC linearity would be lessened by mismatches [10]: mismatches of the charges injected from S_4 and S_3 and mismatches of capacitors C_1 and C_2.

B. Settling Time

The simplified CMC schematic shown in Fig. 7(b) [small-signal schematic (C_{gd} is neglected)] can be used to approximate the time constant of the DME-CMC. Assuming that $G_{ds} \ll g_m$ and $G_{ds} \ll G_{\rm on}$, and neglecting the s^3 terms

$$\frac{i_{\rm out}}{i_{\rm in}} = \frac{1 + \frac{C_1}{G_s}s}{1 + \left(\frac{C_1}{G_s} + \frac{C_1 + C_d + C_3}{g_m}\right)s + \left(\frac{(C_1+C_3)C_d}{g_m G_{\rm on}} + \frac{C_1(C_d+C_3)}{g_m G_s}\right)s^2}$$

(where $i_{\rm out}$ is equal to $g_m v_g$), a global settling time constant may reasonably be approximated by $10\,\tau \approx 16.5$ ns, where $\tau \approx (C_1 + C_d + C_3/g_m)$, and C_d is the CMC input parasitic capacitor ($C_1 = 0.6$ pF, $C_3 = 0.25$ pF, and $C_d \approx 0.3$ pF). Simulations give 15.5 ns for a 200-μA input step transition to achieve 13-bit accuracy and 22 ns for a 200-μA transmission current between two CMCs. Acquisition time $t_{\rm ac}$ is thus about 25 ns, which theoretically implies a 20-MS/s sampling frequency. To reduce $t_{\rm ac}$, C_3 (C_4) can be lowered (thus increasing the open-loop gain of the Opamp to keep the same resolution), or the g_m can be increased.

C. Opamp Bandwidth

For the purpose of using this DME-CMC in current-pipelined ADCs [2], which are made up of two CMCs per stage, the Opamp settling time should be lower than $t_{\rm ac}/2$, so that comparisons of the current memorized by one of the CMCs could take place while the other CMC is sampling the input signal. Consequently, the Opamp settling time has been chosen to be less than 10 ns.

The following equations give an assessment of the Opamp bandwidth that is required to reach the desired settling time. According to (1)

$$\Delta V_{\rm inj}(s) = \frac{\Delta q(s)}{2\left(1 + \frac{A_d(s)}{2}\right) \cdot C_3}$$

with

$$A_d(s) = \frac{A_{d_0}}{1 + \tau_{\rm Opamp}\, s}$$

where A_{d_0} stands for the dc open-loop gain of the Opamp, $\tau_{\rm Opamp}$ is the Opamp main time constant, and $\Delta q(s)$ is

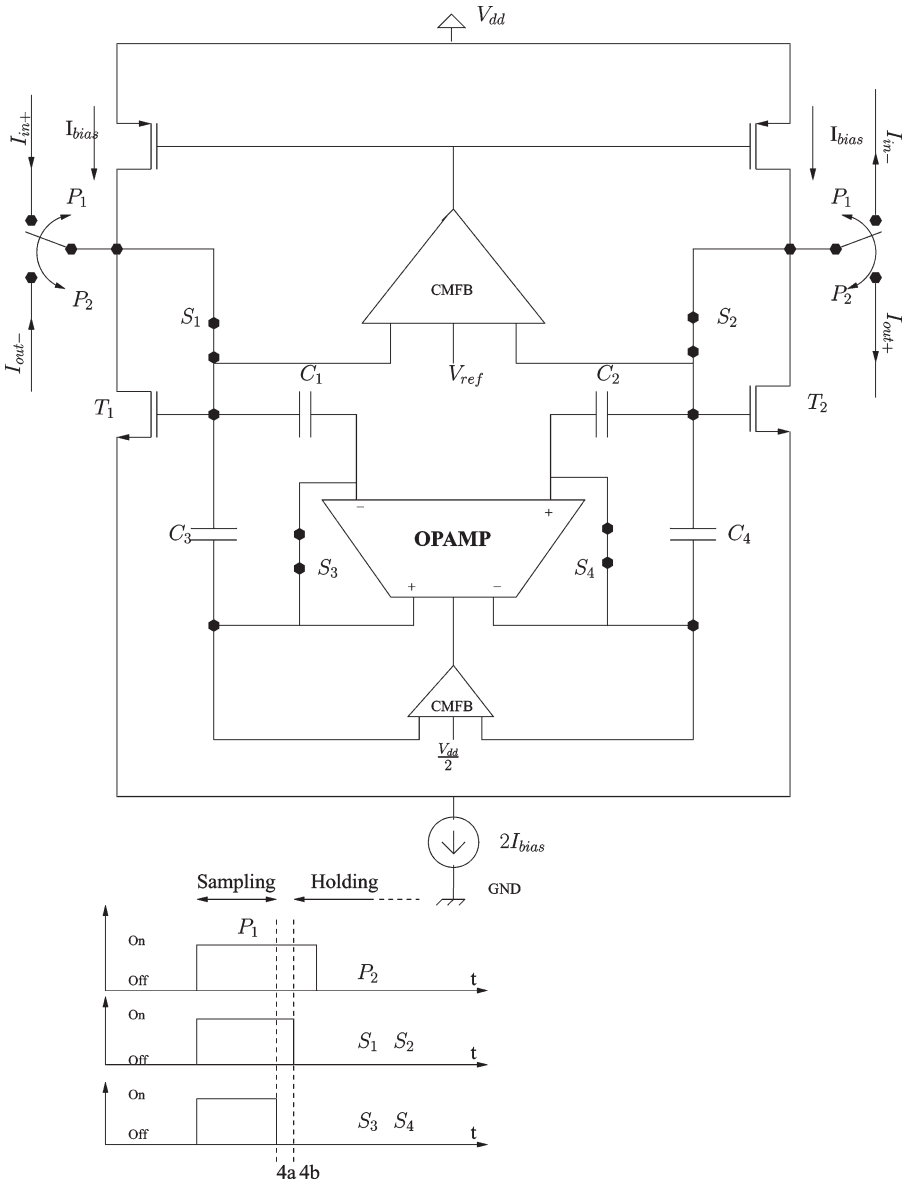

Fig. 5. Fully DME-CMC.

the injected charges ($\Delta q(s) = \Delta q_{\max}/s = C_3 \Delta V_{\mathrm{inj}_{\max}}/s$). Therefore, $\Delta V_{\mathrm{inj}_{\max}}$ is the maximum error voltage without Miller effect. As the Opamp exhibits a first-order filter behavior, its time constant τ_{Opamp} should fulfill the following relationship:

$$\tau_{\mathrm{Opamp}} \leq \frac{(1+A_{d_0})t_{\mathrm{ac}}}{\ln\left(\frac{A_{d_0}}{\gamma(1+A_{d_0})-1}\right)} \quad \text{with} \quad \frac{\Delta V_{\mathrm{inj}}(t)}{\Delta V_{\mathrm{inj}_{\max}}} = \gamma. \qquad (3)$$

According to (3), for a $(1/\gamma) = 100$ charge-injection reduction ratio, the Opamp gain-bandwidth product should be higher than 70 MHz, so that the acquisition time could be lower than 10 ns. Hence, as it can be seen, the design of this Opamp is not an issue, and it has no stability problem linked to its use inside the CMC, as in [5]. Moreover, large input and output voltage swings are not needed. The Opamp structure is based on a fully differential folded cascode architecture (see Fig. 8), which can drive capacitive loads. It was designed to achieve a 60-dB gain and a gain-bandwidth product frequency that is equal to 250 MHz (to allow a larger charge-injection reduction ratio) with a safe phase margin of 80°.

D. CMC Noise

During the CMC operation, the input current signal, as well as noise, is sampled on one clock phase and then held on the other. Among the different kinds of noise, thermal noise is the main source of noise [flicker noise is removed by the sampling process (at high frequency)]. As a consequence, the CMC noise can be approximated by

$$\overline{I}^2_{\mathrm{noise}} \approx \alpha_{\mathrm{diff}} \frac{8}{3} k_B T (g_{m_{\mathrm{Tm}}} + g_{m_{\mathrm{Tbias}}}) \mathrm{BW}_n$$

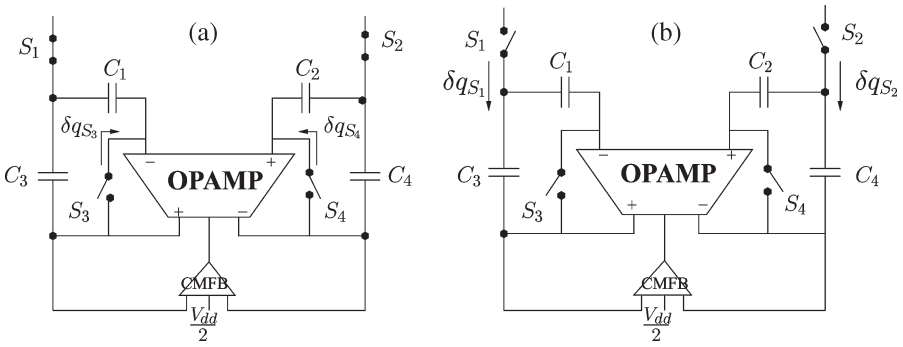

Fig. 6. Miller enhancement circuitry. (a) Switches S_3 and S_4 are turned off to enable the Miller effect. (b) Switches S_1 and S_2 are opened to sample input signals.

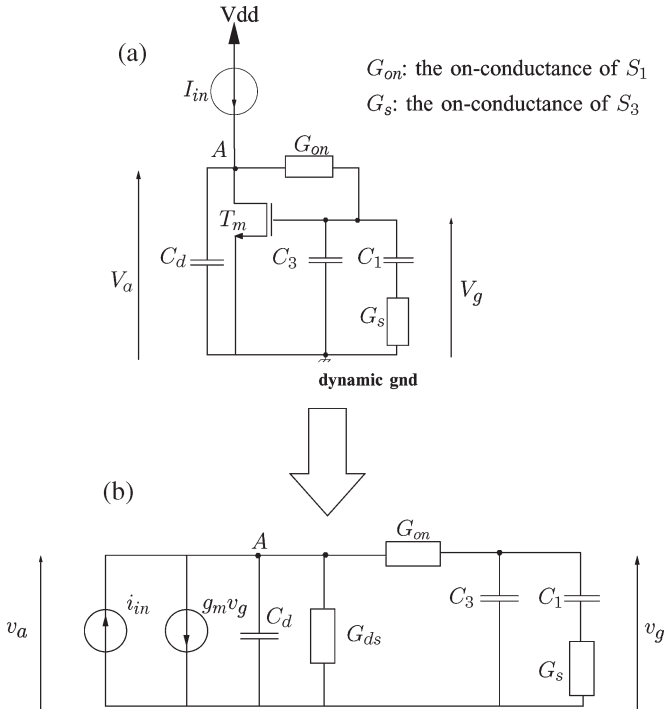

Fig. 7. Settling time assessment, where $i_{\rm in}$ is the input current to be stored, $g_m v_g$ is the output current, $G_{\rm on}$ is the ON-conductance of S_1 (S_2), G_s is the ON-conductance of S_3 (S_4), G_{ds} is the output conductance of transistor T_m, and C_d is a parasitic capacitance.

where k_B is Boltzmann's constant, $g_{m_{\rm Tm}}$ is the T_m transconductance (see Fig. 4), $g_{m_{\rm Tbias}}$ is the $T_{\rm bias}$ transconductance, $\rm BW_n$ is the equivalent noise bandwidth, and $\alpha_{\rm diff} = 2$ (the CMC architecture is differential). By approximating the CMC function transfer by a first-order, low-pass filter, $\rm BW_n$ is given by

$$\rm BW_n = \frac{\pi}{2} \frac{1}{2\pi \left(\frac{C_{gs}+C_d}{g_{m_{Tm}}} \right)}.$$

Therefore, the CMC noise can be written as

$$\overline{I}^2_{\rm noise} \approx \frac{4}{3} k_B T (g_{m_{\rm Tm}} + g_{m_{\rm Tbias}}) \frac{g_{m_{\rm Tm}}}{C_{gs}+C_d}$$

where C_{gs} is the holding capacitor. Note that the Miller effect enhancement is not taken into account in this noise study, contrary to [12]. The signal-to-noise ratio (SNR) is about 62 dB. This SNR is relatively low compared to switched-capacitor circuit performances. This is one of the main weaknesses of *current-mode* circuits. However, due to CMOS process evolution, such circuits may outperform *voltage-mode* circuits, as suggested in [14].

IV. Rad-Hard Implementation and Simulation/Experimental Results

A. Rad-Hard Implementation

The fully differential CMC was designed and implemented in 0.35-μm CMOS technology. The 220×190 μm CMC microchip is shown in Fig. 9. This CMC and its test circuits (see Fig. 10) have been implemented together within a 2×2 mm microchip. These embedded test circuits allow one to directly measure the T_m gate voltage through output buffers (300-MHz bandwidth) and the output current held by the CMC, as well as the reference currents through transimpedance amplifiers (see Fig. 10). In addition, it is possible to enable or disable the Miller effect enhancement.

Furthermore, some special design and layout considerations were implemented for the purpose of MOS device and circuit radiation-hardening.

- An enclosed n-channel MOS (NMOS) layout is used to reduce leakage currents [15]. The main disadvantages related to this layout technique are the increase in the gate and source or drain capacitances and the limitations in the choice of the W/L ratio.
- Switches are based on PMOS devices to reduce leakage currents caused by space radiations without using an enclosed configuration so that dummy switches can be used without W/L ratio constraints.
- Guard rings are always used to prevent latchup events.

B. Simulation/Experimental Results Prior to Irradiation

Since such a kind of sample-and-hold should deal with large changes in input levels between sampling instants (CCD input signal), the input signals generated by the test structure are

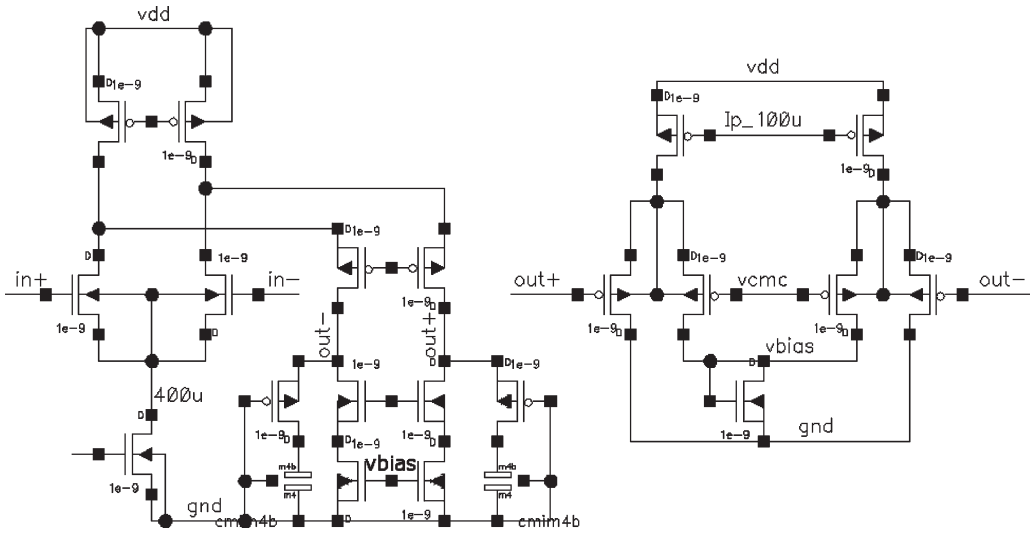

Fig. 8. Circuit schematic of the Opamp with its CMFB circuit.

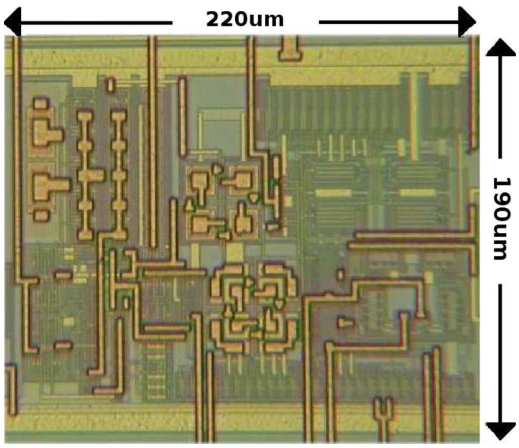

Fig. 9. CMC microchip.

square waves. Consequently, to test the CMC response to sinus waves, on account of the ON-chip test bench, it is necessary to modulate all the microchip currents (bias currents, as well as input signal currents), which implies that a direct measurement of the CMC linearity based on sinus wave input is not possible. The waveform for the DME-CMC to sample and hold a 800-kHz sinusoidal input signal with a peak-to-peak amplitude of 80 μA (which means a $\pm 20\%$ current modulation) at a 5.8-MHz clock rate is shown in Fig. 11. The measured acquisition time for a 200-μA step transition to 0.1% accuracy is approximately 50 ns, which is different from the 25-ns expected acquisition time. It can be explained by the parasitic capacitances induced by the output voltage buffers (see Fig. 10).

The output current error induced by charge injections can be assessed by measuring the gate voltage of the memory transistors via the output voltage buffers. Indeed, (2) can also be written as follows for a symmetric differential architecture (it is assumed that this differential error is small compared to the ideal differential voltage held between T_{m_1} and T_{m_2}):

$$\Delta I_D \approx \frac{g_{m_1} + g_{m_2}}{2} \Delta V_{\text{inj}} \tag{4}$$

where g_{m_x} is the transconductance of T_{m_x}, the value of which depends on the current held, and ΔV_{inj} is the differential gate voltage error due to charge injections. Furthermore, based on [4], ΔI_D can also be approximated by

$$\Delta I_D \approx \sqrt{\frac{2I_{\text{bias}}}{\beta}} (\sqrt{1+m} + \sqrt{1-m}) \frac{\Delta V_{\text{inj}}}{2} \tag{5}$$

$$\approx \sqrt{\frac{2I_{\text{bias}}}{\beta}} \left(1 + \frac{\Delta V_{\text{inj}}}{8} + o(m)\right) \Delta V_{\text{inj}}. \tag{6}$$

Without the Miller effect (Fig. 12), the CMC accuracy is lower than 6 bits since $\Delta V_{\text{inj}_{\max}} \approx 5.74$ mV [for $V_{\text{diff}}^{\max} = 250$ mV (corresponding to a 200-μA input current signal)]. As far as nonlinearity is concerned, the maximum measured deviation ΔV_{inj} from the V_{inj} linear regression curve is ± 75 μV ($\pm 2.7\%$). According to (5), it is equivalent to a $\pm$80-nA nonlinearity error (for $m = 0.4$) or approximately 11.3-bit resolution.

When the Miller effect is enabled, the maximum error voltage is lower than 250 μV. It implies that the measured accuracy of the DME-CMC is 10 bits. Similarly, the maximum measured deviation ΔV_{inj} (for $m = 0.4$) from the V_{inj} linear regression curve is 45 μV, which implies a 50-nA nonlinearity error or approximately 12-bit resolution. Furthermore, note the presence of a 4-mV offset (Fig. 12 and Table I). This offset is not present when the Miller effect is disabled, which implies that this offset arises from the S_3 and S_4 switches (see Fig. 6), as well as from the clock circuitry scheme. As shown in Table I, this offset is almost the same for the six tested microchips. Therefore, this offset should mainly be due to clock circuitry layout asymmetry.

In addition, the Miller effect enhancement is lower than expected. Indeed, the charge-injection phenomenon is reduced by a 23-time factor, whereas the dc open-loop gain of the Opamp is 60 dB (typical value). To explain the difference, parasitic capacitances should be taken into account. The Opamp

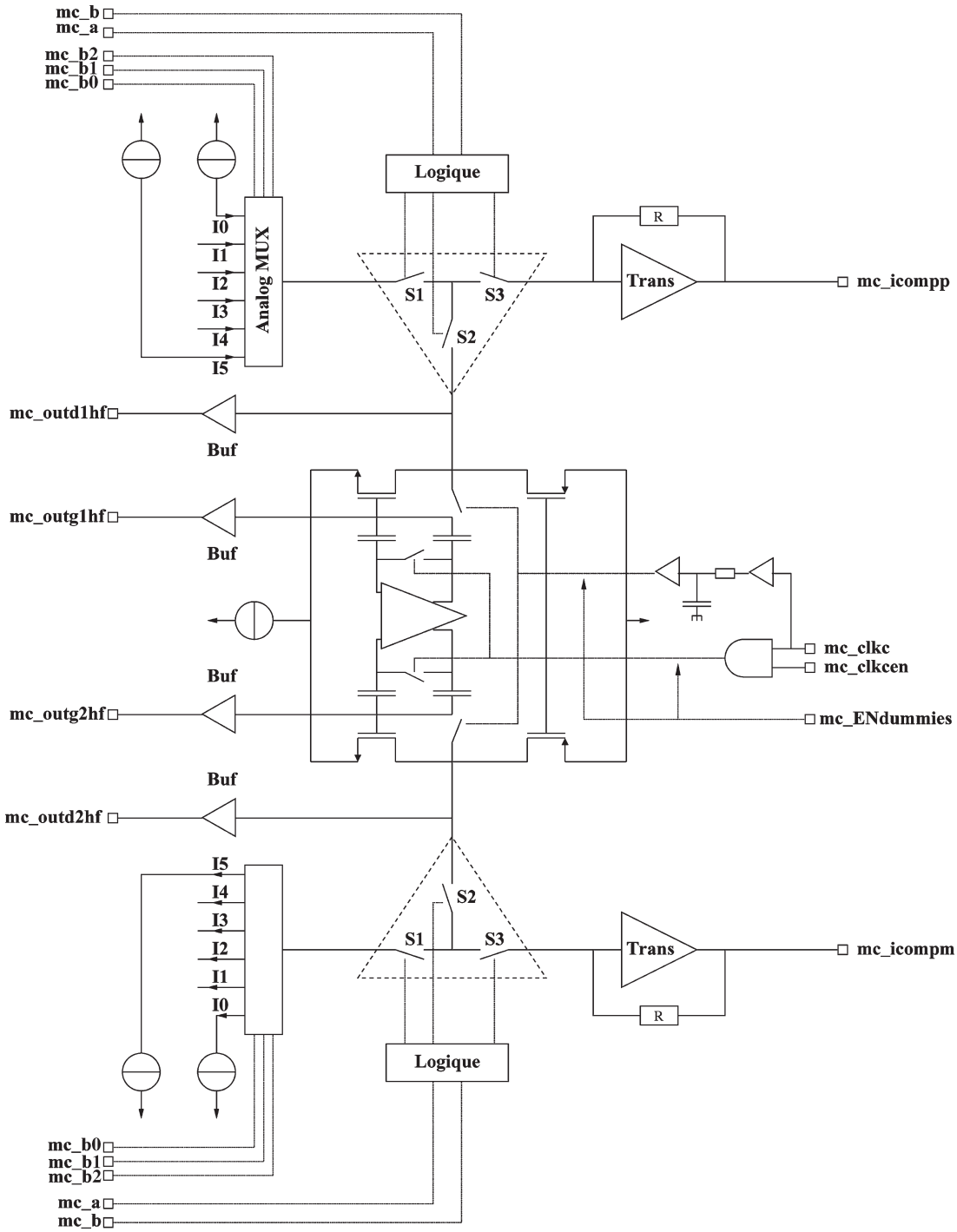

Fig. 10. Synoptic of the CMC ON-chip test bench. Output buffers are used to probe T_m gate voltage and the output voltage of the CMC. Output transimpedances directly probe the output current from the CMC and the reference currents.

and switch parasitic capacitances C_{o1} and C_{o2} are represented in Fig. 13. Taking into account these parasitics, (1) becomes

$$\Delta V_{\text{inj}} = \frac{\Delta q}{2\left(C_3 + C_1 + \frac{(A_d/2)C_3 - C_1}{C_{0_1}+C_1+(1+A_d/2)C_{0_2}}C_1\right)}. \quad (7)$$

Therefore, according to (7), Miller capacitance C_{Miller} is reduced by parasitic term ς, i.e.,

$$C_{\text{Miller}} \approx \frac{(1+A_d/2)C_3}{\varsigma} \quad (8)$$

where $\varsigma = C_1/(C_1 + (1+A_d/2)C_{0_2})$ (C_{0_1} is neglected). Consequently, if $A_d \gg 1$

$$\Delta V_{\text{inj}} = \frac{\Delta q}{C_3\left(1+\frac{C_1}{C_{0_2}}\right) + C_1}.$$

This term ς can thus be large, even if C_{0_2} is small, and the Miller effect gain can be approximated by the ratio C_1/C_{0_2}. Spice simulations, which take into account those CMC parasitic capacitances (see Table II), agree with the theoretical analysis.

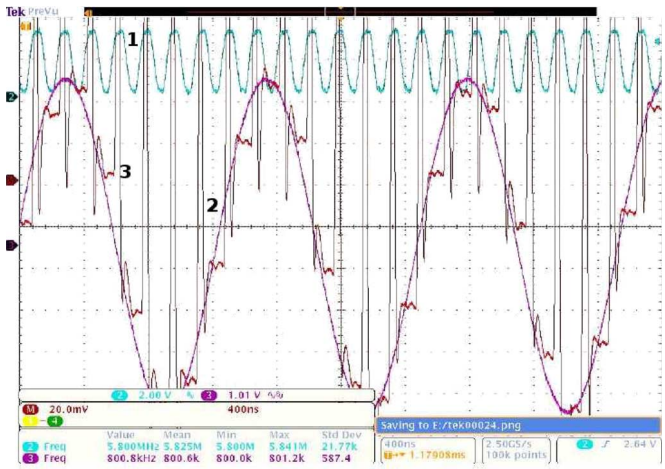

Fig. 11. Measured waveforms of the DME-CMC. The output signal (3) is obtained by sampling and holding a 800-kHz sinusoidal input signal (2) with a peak-to-peak amplitude of 80 μA at a 5.8-MHz clock rate (1).

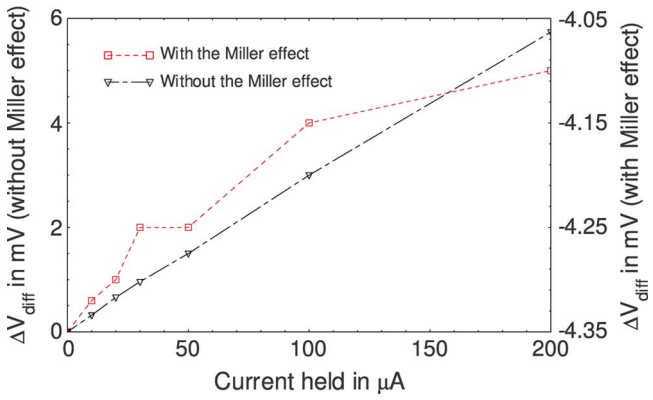

Fig. 12. Measured differential voltage error $\Delta V_{\rm inj}$ of the memory transistor T_{m_x} due to charge injections (with and without the Miller effect enabled).

TABLE I
$\Delta V_{\rm inj}$ MEASURED OFFSET WITH MILLER EFFECT ON SIX MICROCHIPS

Chip	1	2	3	4	5	6
Offset (mV)	4.7	4.2	4.15	4.25	3.6	4

The estimated equivalent parasitic capacitance of the CMC is 3 fF, which means that the Miller effect is approximately 80 ($\ll$ 1000 Opamp gain). However, the layout parasitic capacitances due to the output voltage buffer are not taken into account, which can explain why the measured gain is only 23.

The experimental performance of the DME-CMC is summarized in Table III, whereas Table IV shows the simulated performances of the DME-CMC used as sample-and-hold. This last set of simulations takes into account mismatches (between the capacitances and the switches used in the Miller effect architecture).

C. Radiation Measurements

To test the radiation tolerance of the CMC, irradiation experiments were carried out on seven chips by using a dedicated machine at ONERA Toulouse. The machine was capable of exposure rates of about 0.05 krad/h. One CMC was used as a control chip (C_1) and, as such, was not irradiated.

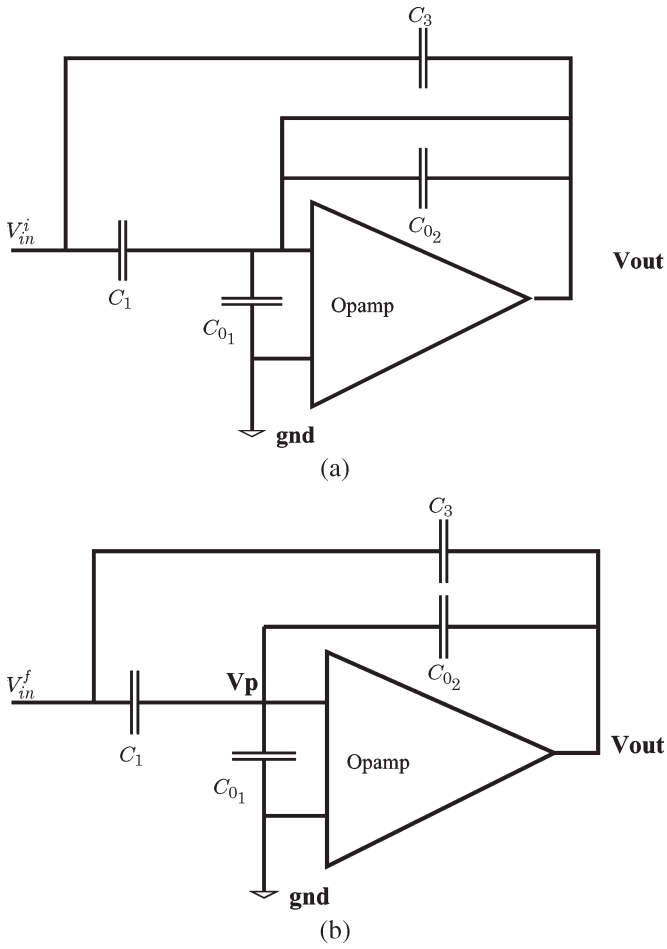

Fig. 13. Miller effect Opamp with its parasitic capacitances. (a) Sampling. (b) Holding.

TABLE II
ASSESSMENT OF PARASITIC CAPACITANCE C_{0_2} VIA CMC SIMULATIONS FOR DIFFERENT (C_1, C_3) VALUES

	ΔV_{inj}	δq_{inj}	C_{0_2} evaluated
(C_1 , C_3)=(0.25pF,0.6pF)	14μV	0.410fC	4.8fF
(C_1 , C_3)=(2.5pF,0.6pF)	3μV	0.491fC	5fF
(C_1 , C_3)=(0.25pF,6pF)	0.9μV	0.8fC	1.5fF

TABLE III
MEASURED PERFORMANCE OF THE DME-CMC

	Theory	Test	
		No Miller	Miller
Power supply	$3.3V - 2.8V$	$3.3V$	$3.3V$
Input common mode	$0.8V - 2V$	$0.9V - 2V$	$0.9V - 2V$
CMOS	$0.35\mu m$	$0.35\mu m$	$0.35\mu m$
Current range	$\mp 200\mu A$	$\mp 200\mu A$	$\mp 200\mu A$
I_{bias}	$250\mu A$	$250\mu A$	$250\mu A$
Settling time	$22ns$	50ns	50ns
Sampling rate	$20MS/s$	$10MS/s$	$10MS/s$
Accuracy $\frac{1}{2}LSB$	13 bits	<5.7bits	10bits
Estimated non-linearity error		$\pm$ 80nA	$\pm$ 50nA
Miller gain	700	0	20 << 40
Current output gain	1	1.02	1.0009
Power	6mW	3mW	6mW
Active Area (μm^2)	-	220 × 190	220 × 190

TABLE IV
SIMULATED SIGNAL-DEPENDENT CHARGE INJECTION FOR INPUT CURRENT RANGING [−200 μA; 200 μA]

Circuit	Current error due to charge injection in μA	Accuracy bits
basic CMC	∓ 6	5
DME-CMC without Miller effect	∓ 0.26	8
DME-CMC	∓ 0.0058	15
DME-CMC with 10% mismatch	∓ 0.02	13

TABLE V
EVOLUTION OF THE TOTAL CURRENT CONSUMPTION FOR THE FIVE CHIPS BIASED UNDER RADIATIONS

	Initial	10krad	30krad	50krad	A_1	A_2
current mA	112	112	111	111	110	101

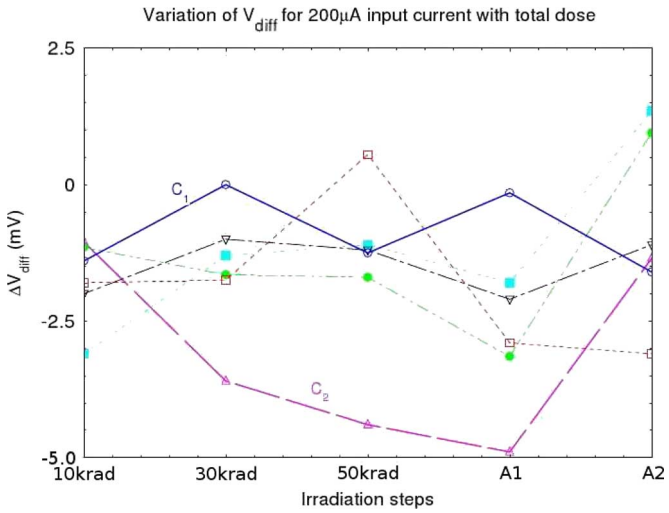

Fig. 14. Variation of V_{diff} for 200-μA input current during irradiation experiments. (1) 10 krad, (2) 30 krad, (3) 50 krad, (4) A_1, and (5) A_2.

Irradiations were carried out in five steps: 10 krad, 30 krad, 50 krad, 24-h annealing (A_1) at 25 °C, and 168-h annealing (A_2) at 100 °C. During each step, all the CMCs were biased except for one C_2 (used also as a control chip), and the clock rate was set at 100 kHz. The absence of any increase in power consumption with total dose confirms on a full circuit scale that enclosed NMOS devices and guard rings prevent radiation-induced leakage (see Table V). During A_2, the measurement is performed at 100 °C, which explains the lower current consumption. Furthermore, all the chips remain fully functional, and no latchup was observed. Fig. 14 shows that radiation-induced transistor parameter shifts are reduced by the use of submicrometer CMOS technologies.

V. CONCLUSION

This paper describes a rad-hard differential CMC, which is based on the Miller effect. Charge-injection errors can be reduced by a factor of 23 at least by using this fully differential charge-injection attenuation architecture. It has also been shown that the parasitic capacitances within the amplifier used to create the Miller effect are the major limitations of this technique. The DME-CMC implemented can achieve an accuracy of 10 bits and an estimated ±50-nA nonlinearity error at a 10-MS/s sampling rate, even if large PMOS switches are used for radiation purposes. Finally, it was shown that such a DME-CMC can sustain 50-krad total dose radiation without failure. The presented CMC results prove that such an architecture is very promising for the implementation of a low-voltage, rad-hard pipelined ADC for space applications in nonradition-hardened CMOS process.

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